



MS-7599 VER:1.0

CPU

AMD AM3 Socket 941

System Chipset

AMD RX780

ATI SB710/700/750

On Board Chip

FINTEK Super I/O -- F71889

LAN -- RTL8111DL

HD Codec --ALC888VC2

BIOS -- SPI ROM 8M

Main Memory

DDR III X 4 (Max 8GB)

Expansion Slots

PCI-E X 16 *1

PCI-E X 1 *2

PCI 2.2 Slot X 3

PWM

Controller--Intersil ISL6323 4+1 Phase

Vcore 4 Phase (MOS HIGHX2 LOWX2)

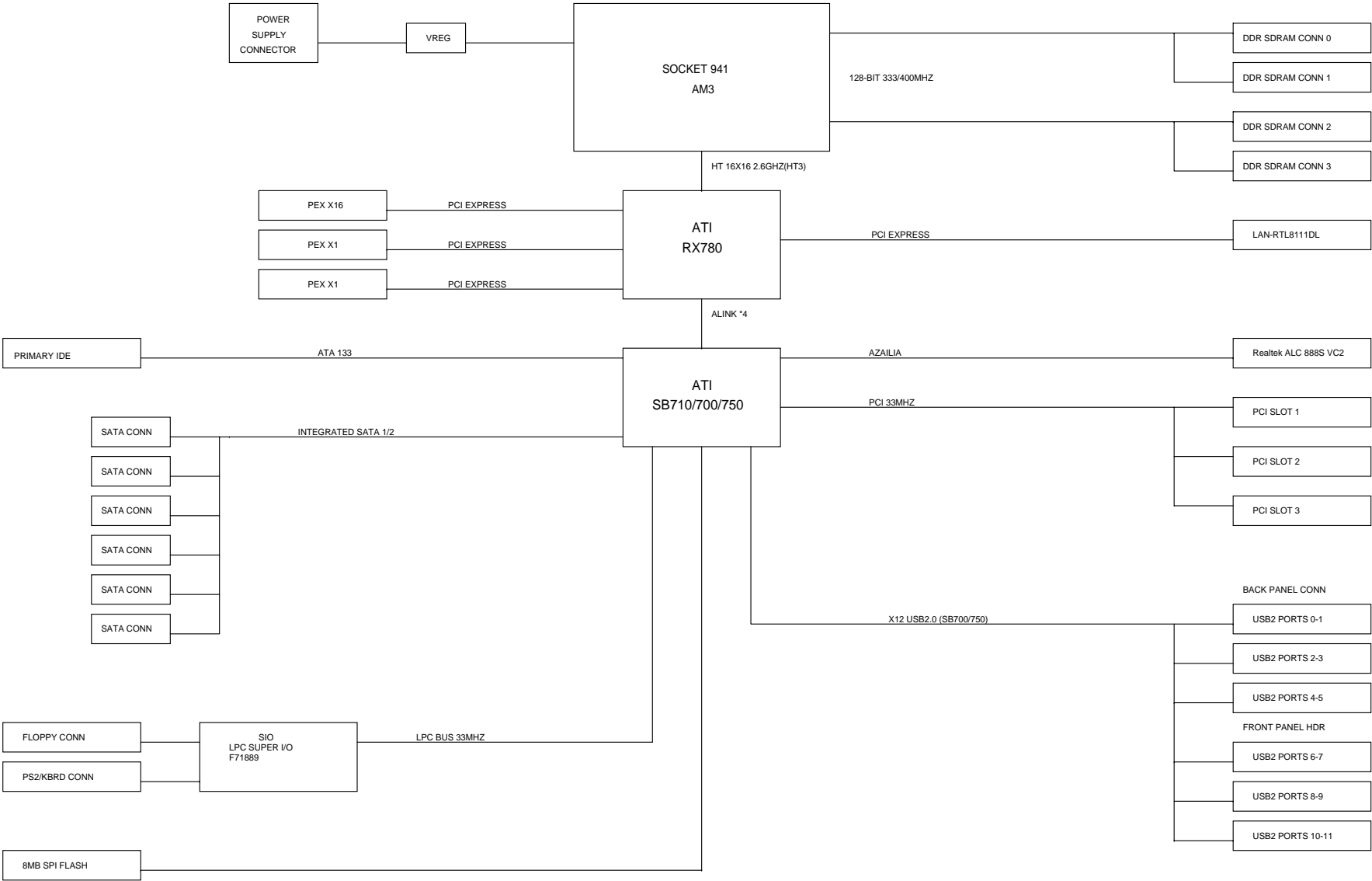
Vnb 1 Phase (MOS HIGHX1 LOWX2)

Clock Generator

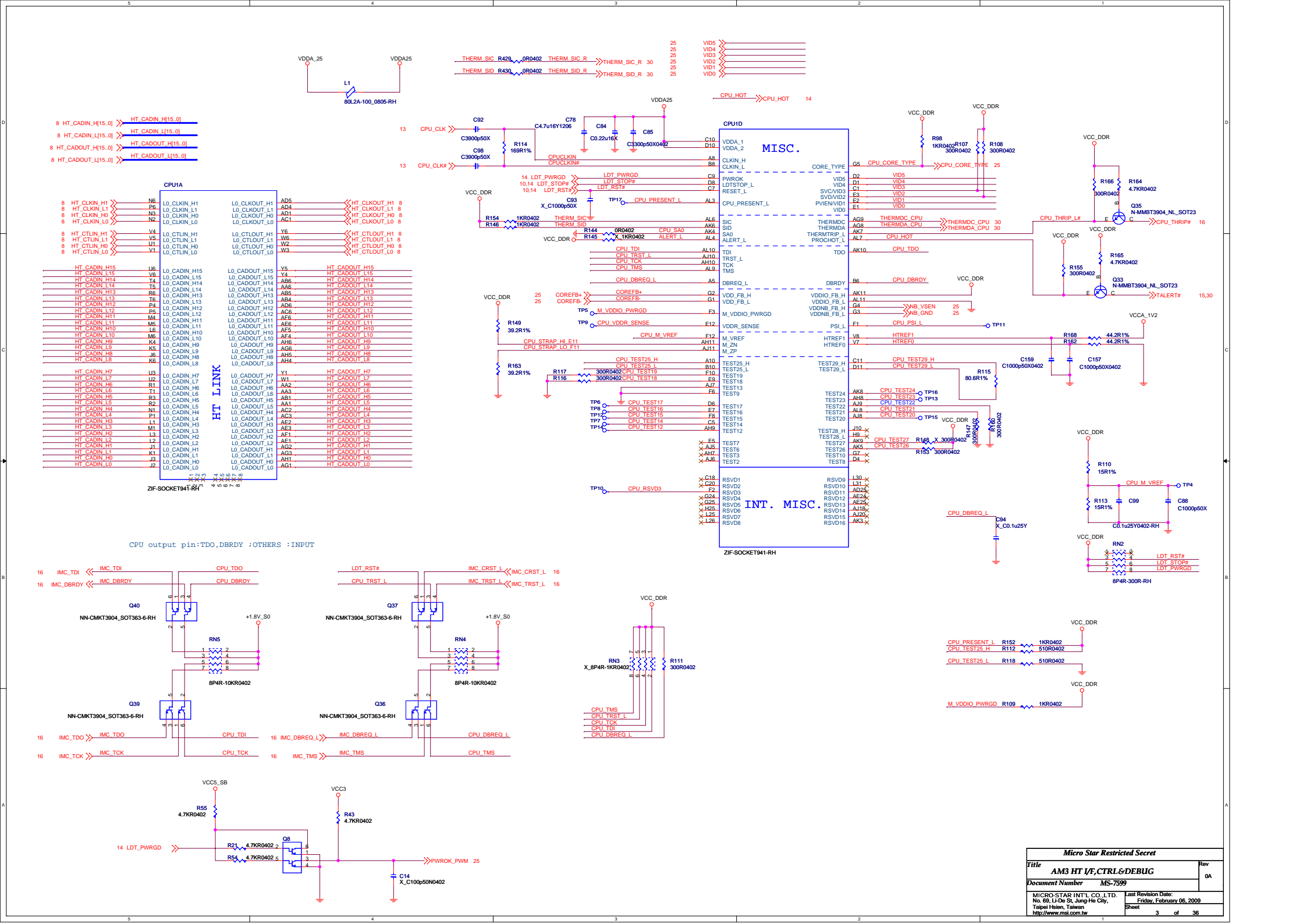
Controller--RTM880N-793

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BLOCK DIAGRAM

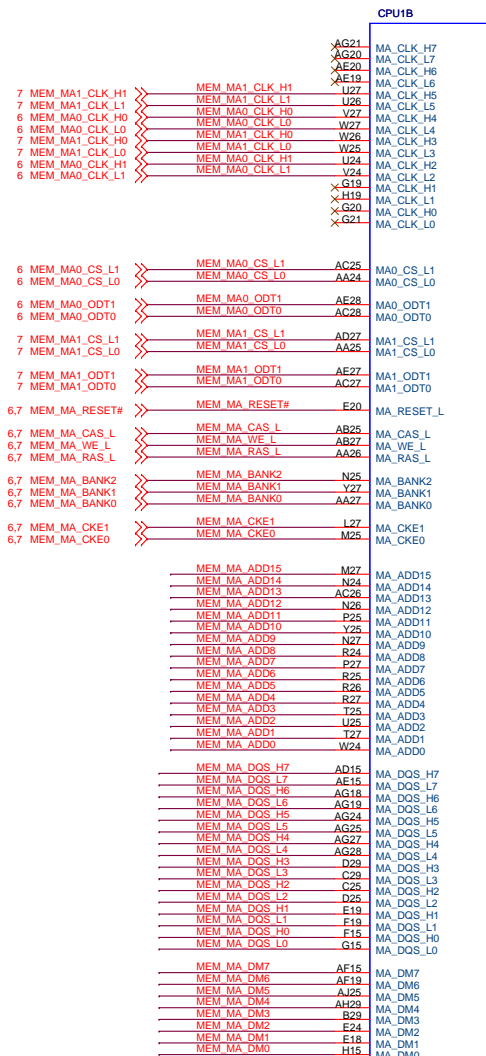


Micro Star Restricted Secret		
Title	Block Diagram	Rev
Document Number	MS-7599	0A
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, February 03, 2009 Sheet 2 of 36

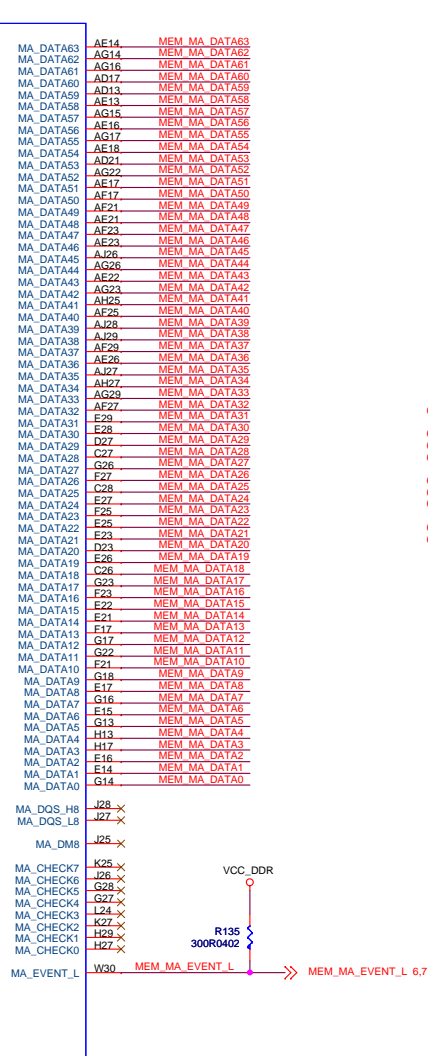


6,7 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
6,7 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
6,7 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
6,7 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
6,7 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]

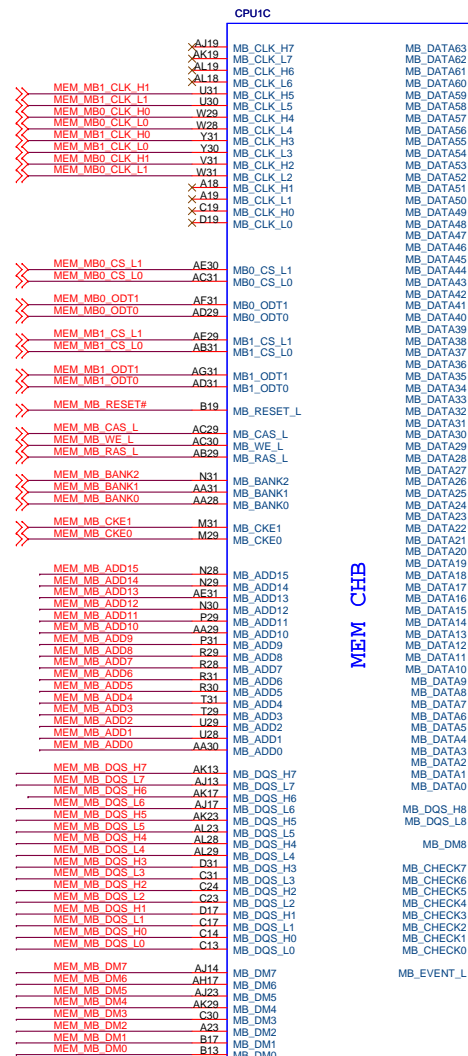
6,7 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
6,7 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
6,7 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
6,7 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
6,7 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]



ZIF-SOCKET941-RH

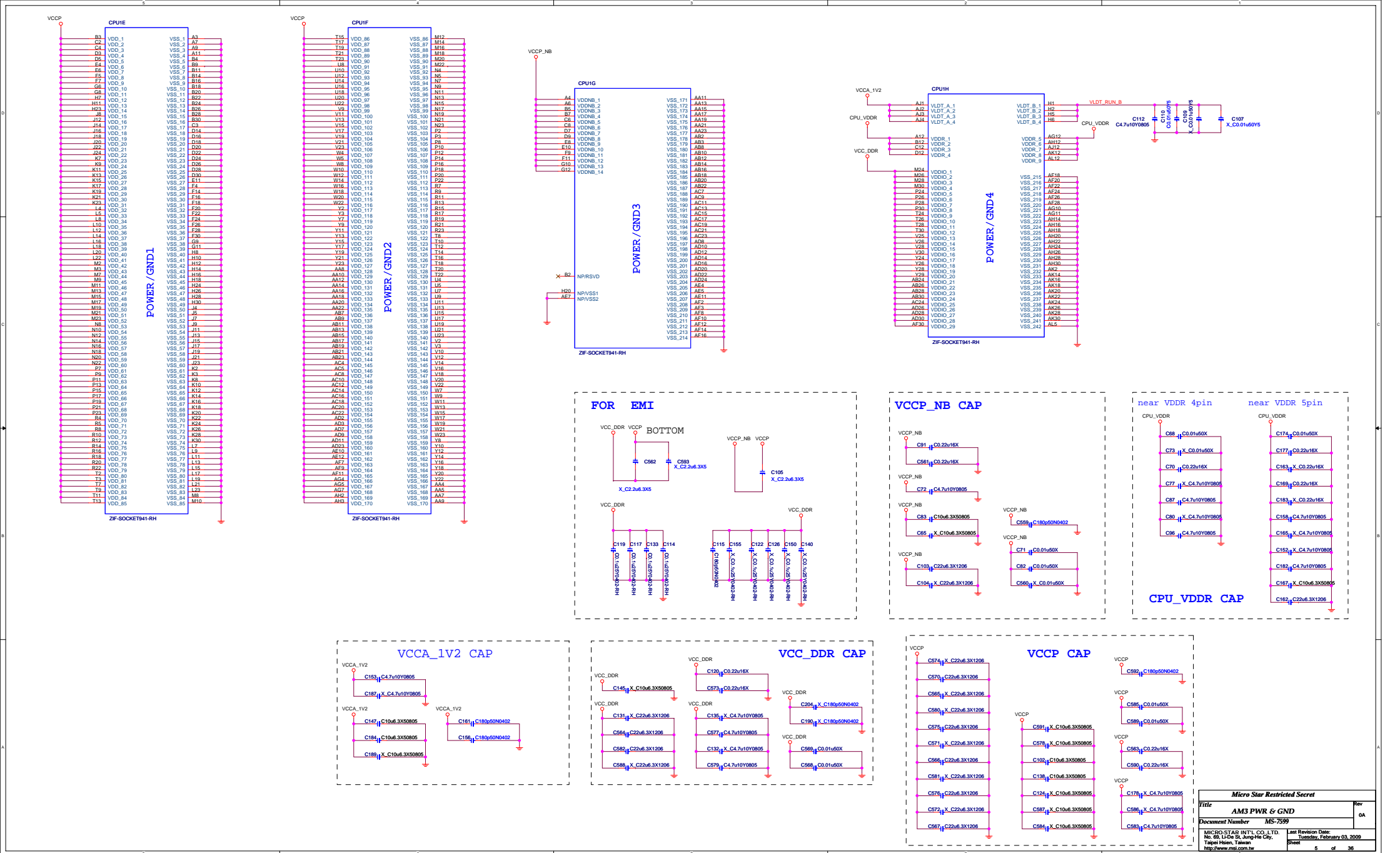


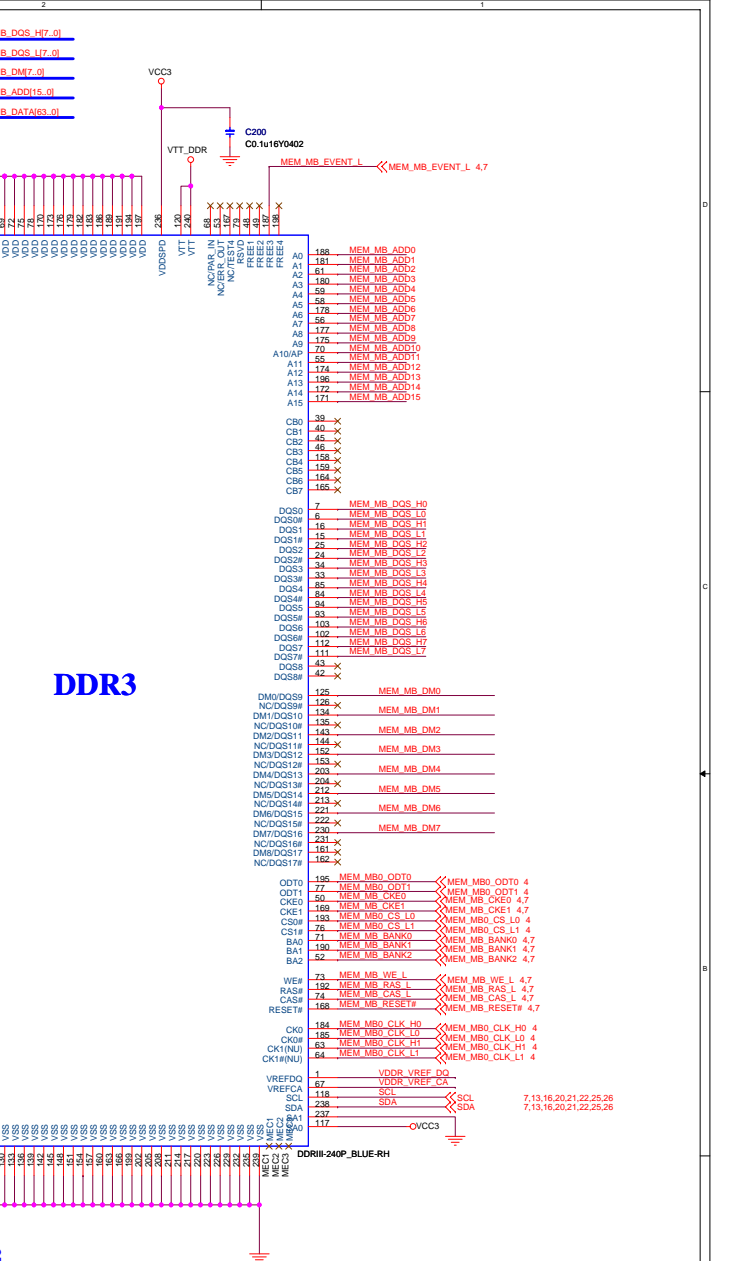
MEM MA EVENT_L



ZIF-SOCKET941-RH

MEM MB EVENT_L

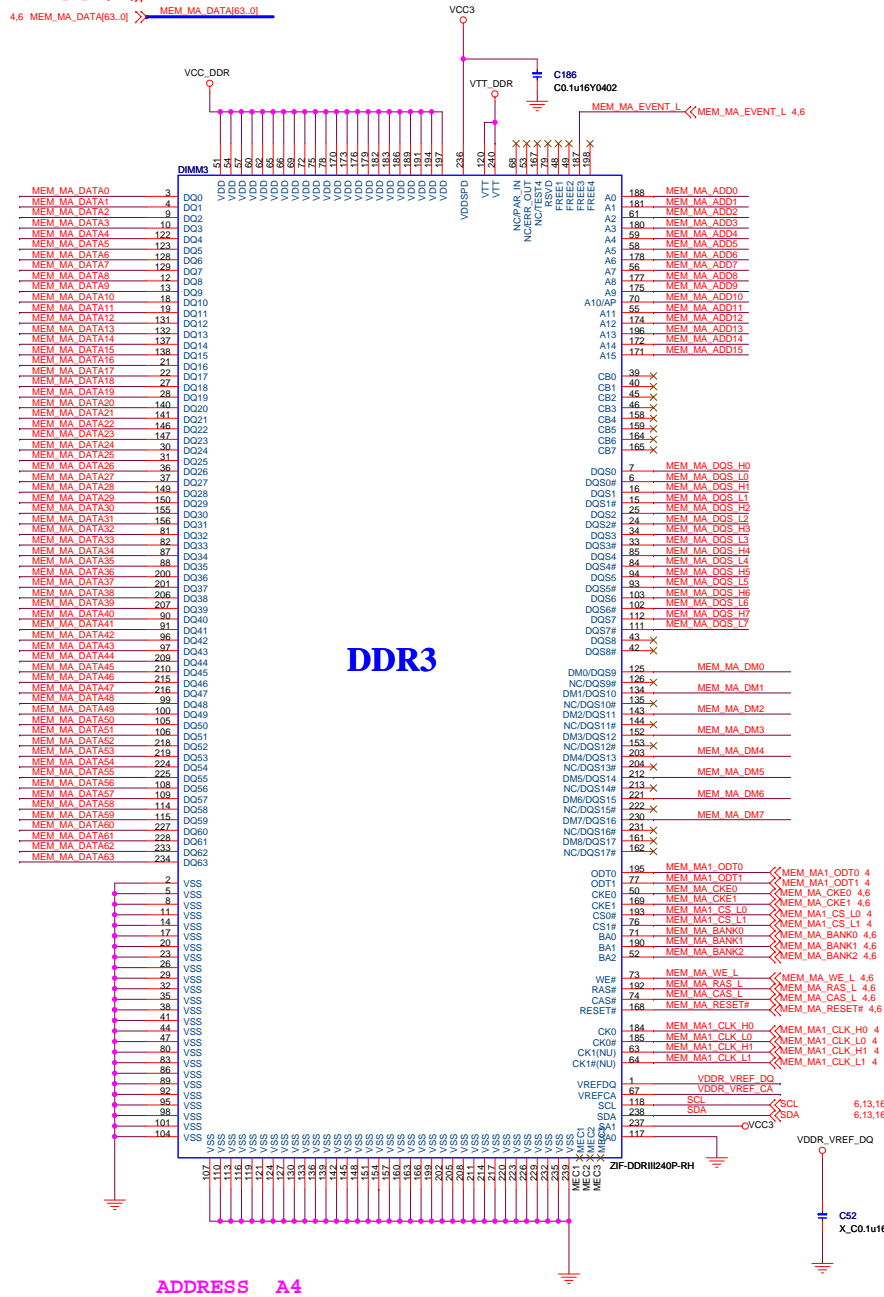




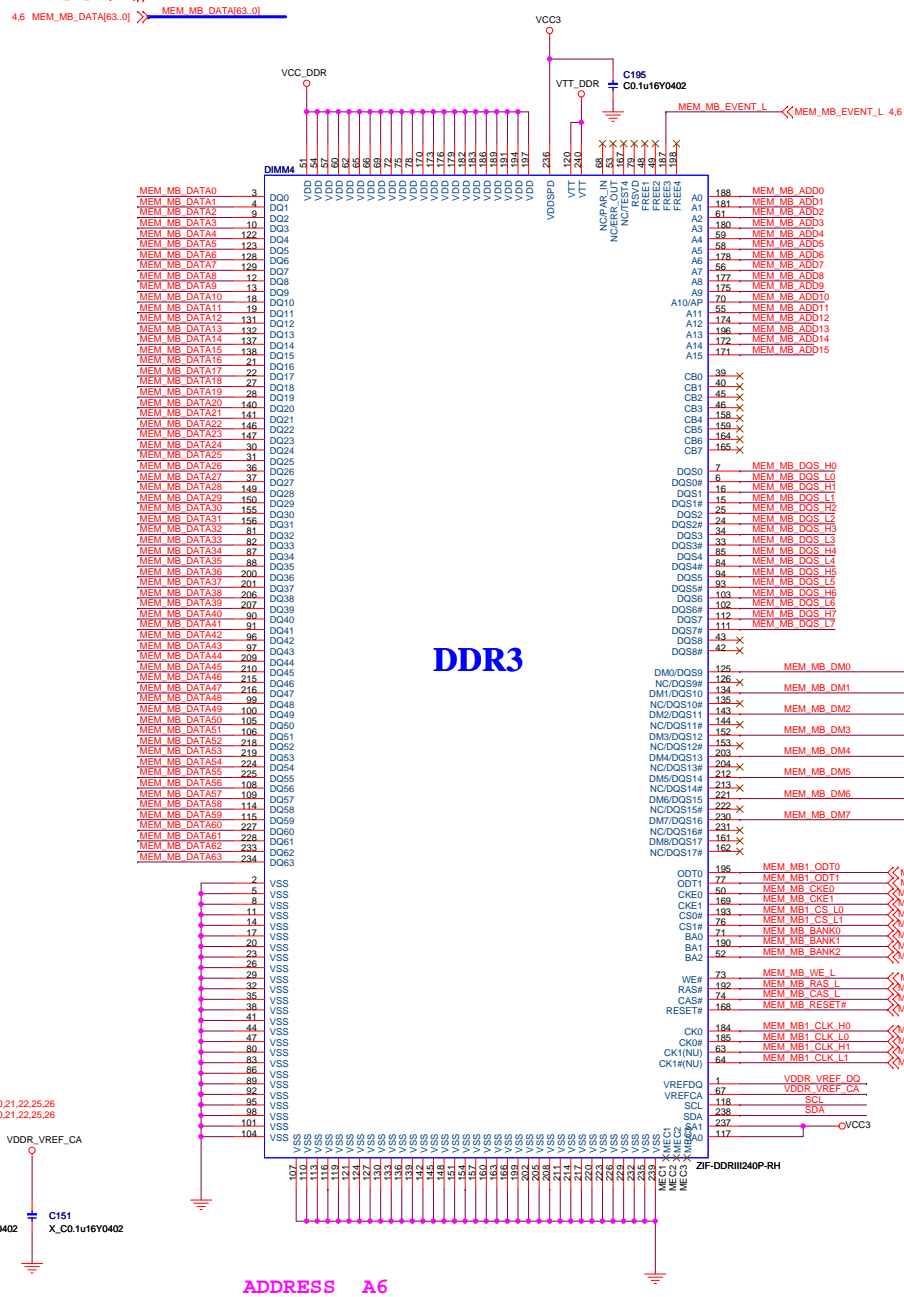
SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMA1	A4
DIMMB1	A6

ADDRESS A2

4.6 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
4.6 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
4.6 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
4.6 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
4.6 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]



4.6 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
4.6 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
4.6 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
4.6 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
4.6 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]

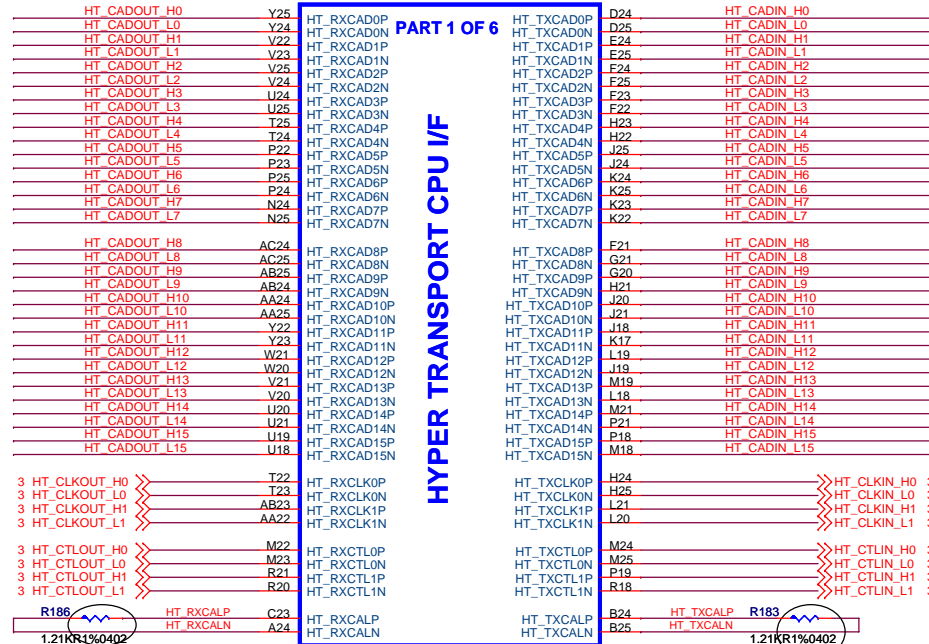


3 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
3 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]
3 HT_CADOUT_H[15..0] >> HT_CADOUT_H[15..0]
3 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]

NB1A

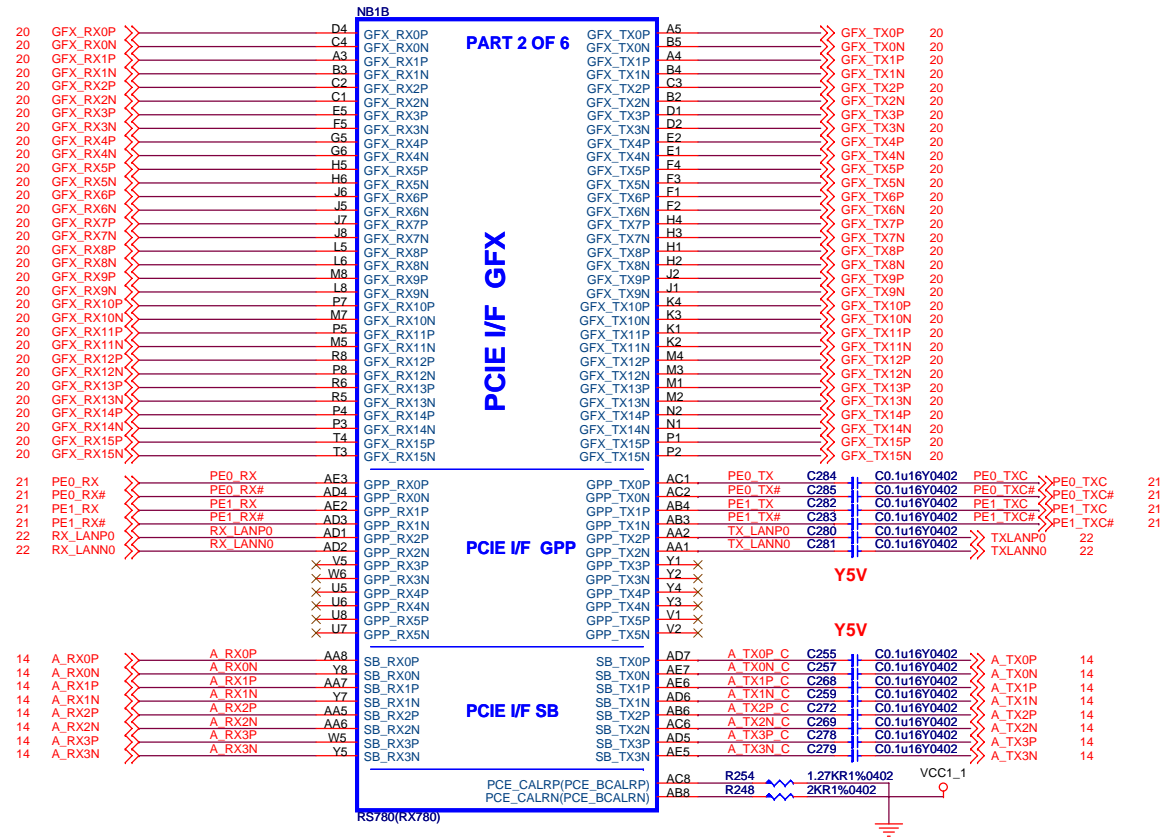
PART 1 OF 6

HYPER TRANSPORT CPU I/F



RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780/RS780
HT_RXCALP	49.9R (GND)	1.21K
HT_RXCALN	49.9R (VDDHT)	
HT_TXCALP	100R	1.21K
HT_TXCALN		

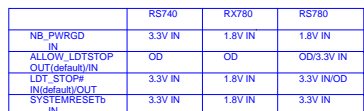


RX740/RS740/RS780 difference table (PCIE LINK)

	RS740	RX740/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1



NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	6M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P				
REFCLK_N	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

PART 3 OF 6		CRTL/ROUT		VLTN		PM PLL PWR		CLOCKS		MIS.													
<p>NRIC</p> <p>X E12 AVDD1(NC)</p> <p>X E12 AVDD2(NC)</p> <p>X E14 AVDD0(NC)</p> <p>X G15 AVSS0(NC)</p> <p>X H15 AVSSQ(NC)</p> <p>X H14 AVSSQ(NC)</p>		<p>TXOUT_L0P(NC) A22 X</p> <p>TXOUT_L0N(NC) B22 X</p> <p>TXOUT_L1P(NC) A21 X</p> <p>TXOUT_L1N(NC) B21 X</p> <p>TXOUT_L2P(NC) B20 X</p> <p>TXOUT_L2N(DBG_GP100) A20 X</p> <p>TXOUT_L3P(NC) B19 X</p>		<p>TXOUT_L0P(NC) A18 X</p> <p>TXOUT_L0N(NC) B18 X</p> <p>TXOUT_U1P(PCIE_RESET_GP103) A17 X</p> <p>TXOUT_U1N(PCIE_RESET_GP103) B17 X</p> <p>TXOUT_U2P(NC) D21 X</p> <p>TXOUT_U2N(NC) D12 X</p> <p>TXOUT_U3P(PCIE_RESET_GP105) A19 X</p> <p>TXOUT_U3N(PCIE_RESET_GP101) B16 X</p>		<p>TXCLK_L1P(DBG_GP101) A16 X</p> <p>TXCLK_L1N(DBG_GP103) B16 X</p> <p>TXCLK_UP(PCIE_RESET_GP104) A16 X</p> <p>TXCLK_UN(PCIE_RESET_GP101) D17 X</p>		<p>VDDLTP18(NC) A13 X</p> <p>VSSLTP18(NC) B13 X</p> <p>VDDL18_1(NC) A15 X</p> <p>VDDL18_2(NC) B15 X</p> <p>VDDL18_3_1(NC) A14 X</p> <p>VDDL18_3_2(NC) B14 X</p>		<p>VSSLT1(VSS) C14</p> <p>VSSLT2(VSS) D15</p> <p>VSSLT3(VSS) E16</p> <p>VSSLT4(VSS) E18</p> <p>VSSLT5(VSS) C20</p> <p>VSSLT6(VSS) E19</p> <p>VSSLT7(VSS) C22</p>		<p>R224</p> <p>R253</p>											
<p>R241 2KR1%0402</p> <p>R250 2KR1%0402</p>		<p>R0780 DFT GP105 E17</p> <p>R0780 DFT GP102 F17</p> <p>R0780 DFT GP104 F15</p>		<p>R0780 DFT GP100 G18</p> <p>R0780 DFT GP101 X G17</p> <p>R0780 DFT GP103 X E18</p> <p>X E19</p>		<p>DAC_HS(NC) A11</p> <p>DAC_VSYNCP(WM_GP106) E8</p> <p>DAC_SDA(PCIE_TCARLN) F8</p> <p>DAC_SCL(PCIE_TCARLN) X G14</p>		<p>DAC_RST(PWM_GP101) A12</p> <p>PLLVD18(NC) B12</p> <p>PLLVD18(NC) X D14</p> <p>PLLVSS(NC) X D12</p>		<p>VDDA18HTPLL H17</p> <p>VDDA18PCIEPLL D17</p> <p>VDDA18PCIEPLL E17</p>		<p>LD1_RST# L D8</p> <p>NB_PWROG_IN A10</p> <p>LD1_STOP# L C10</p> <p>ALLOW_LD1STOP C12</p>		<p>HT_REFCLK# C26</p> <p>HT_REFCLK C24</p> <p>HT_REFCLK F11</p> <p>REFCLK_P10SCIN(OSCIN) X F11</p>		<p>GFX_REFCLK T2</p> <p>GFX_REFCLKN G7</p> <p>GP1P_REFCLK U1</p> <p>GP1P_REFCLKN U2</p> <p>GP1P5B_REFCLKP(SB_REFCLKP) V4</p> <p>GP1P5B_REFCLKN(SB_REFCLKN) V3</p>		<p>I2C_DATA A9</p> <p>I2C_CLK B9</p> <p>DOC_DATA(AUX0P(NC)) X A8</p> <p>DOC_CLK(AUX0P(NC)) X A7</p> <p>AUX1P(NC) X A7</p> <p>AUX1N(NC) X A7</p>		<p>STRP_DATA B10</p> <p>STRP_DATA G11</p> <p>R212</p> <p>R180(RX780)</p>		<p>TESTMODE D13 TEST EN</p> <p>91KR0402</p>	

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable (RS740); Disable(RX780/RS780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

```

111: 1-1-1-1-1-1 Mode L default
110: 1-1-1-1-1-1 Mode L
101: 2-0-2-0-2-0 Mode C2
100: 2-0-2-0-1-1 Mode K
011: 2-0-1-1-1-1 Mode E
010: 1-1-1-1-1-1 Mode L
001: 4-0-0-0-1-1 Mode C
000: 4-0-0-0-2-0 Mode B

```

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
  default values if not connected
RS740: pin DFT_GPI01
RX780: pin DFT_GPI01
RS780: pin SUS_STAT#
```

```
Enables Test debug bus
using PCIe bus
1. Disable (can be enabled
   thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register
      setting only
RS740: Not supported
```

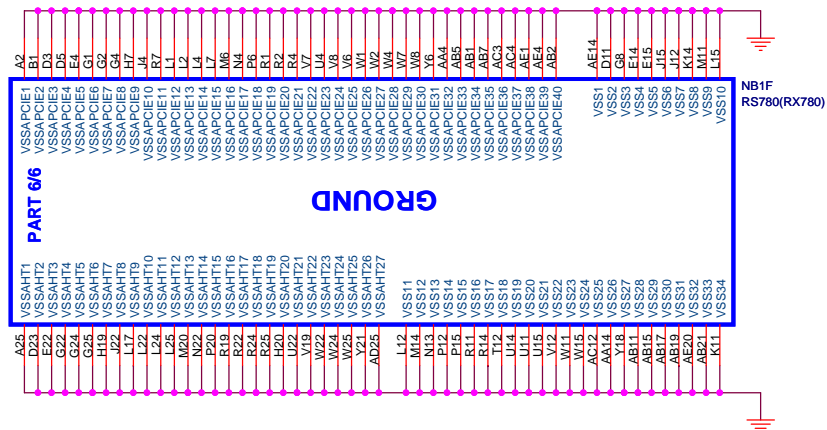
	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

NB1D		PAR 4 OF 6	
AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18
AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20
V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA19
AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19
AA12	MEM_A4(NC)	MEM_DQ4(NC)	Y17
AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17
AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15
AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15
AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20
AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19
AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22
AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18
AC14	MEM_A12(NC)	MEM_DQ12(NC)	AB20
Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22
		MEM_DQ14/DVO_D10(NC)	AC22
		MEM_DQ15/DVO_D11(NC)	AD21
AD16	MEM_BA0(NC)		Y17
AE17	MEM_BA1(NC)		W18
AD17	MEM_BA2(NC)	MEM_DQS0P/DVO_IDCKP(NC)	AD20
		MEM_DQS0N/DVO_IDCKN(NC)	AE21
W12	MEM_RASb(NC)	MEM_DQS1P(NC)	
Y12	MEM_CASb(NC)	MEM_DQS1N(NC)	
AD18	MEM_WEB(NC)		
AB13	MEM_CSB(NC)	MEM_DM0(NC)	W17
AB18	MEM_CKE(NC)	MEM_DM1/DVO_D8(NC)	AE19
Y14	MEM_ODT(NC)		
		IOPLLVD18(NC)	AE23
V15	MEM_CKP(NC)	IOPLLVD(NC)	AE24
W14	MEM_CKN(NC)		
		IOPLLVS(NC)	AD23
AE12	MEM_COMPP(NC)		
AD12	MEM_COMPN(NC)	MEM_VREF(NC)	AE18
RS780(RX780)			

Note: If the Side-port memory interface is **not** used, make sure that:

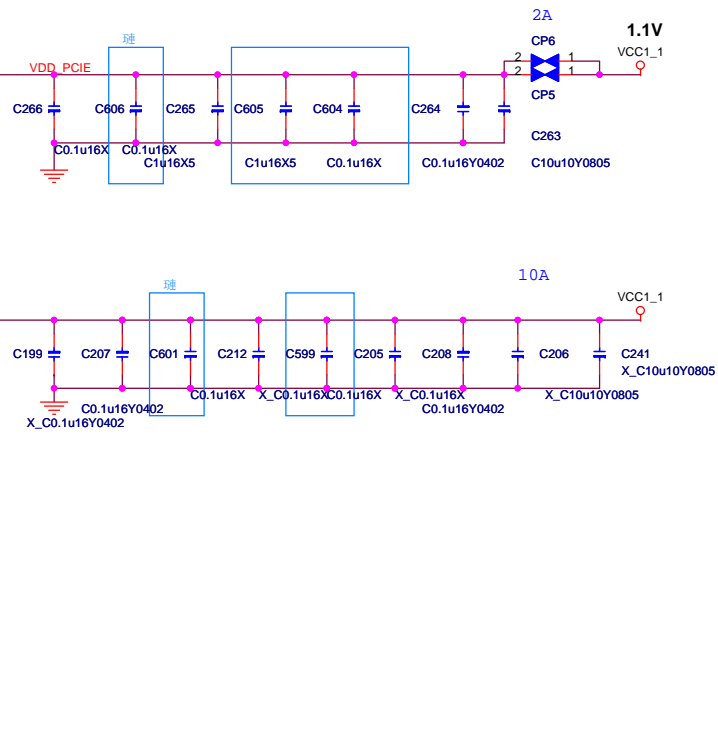
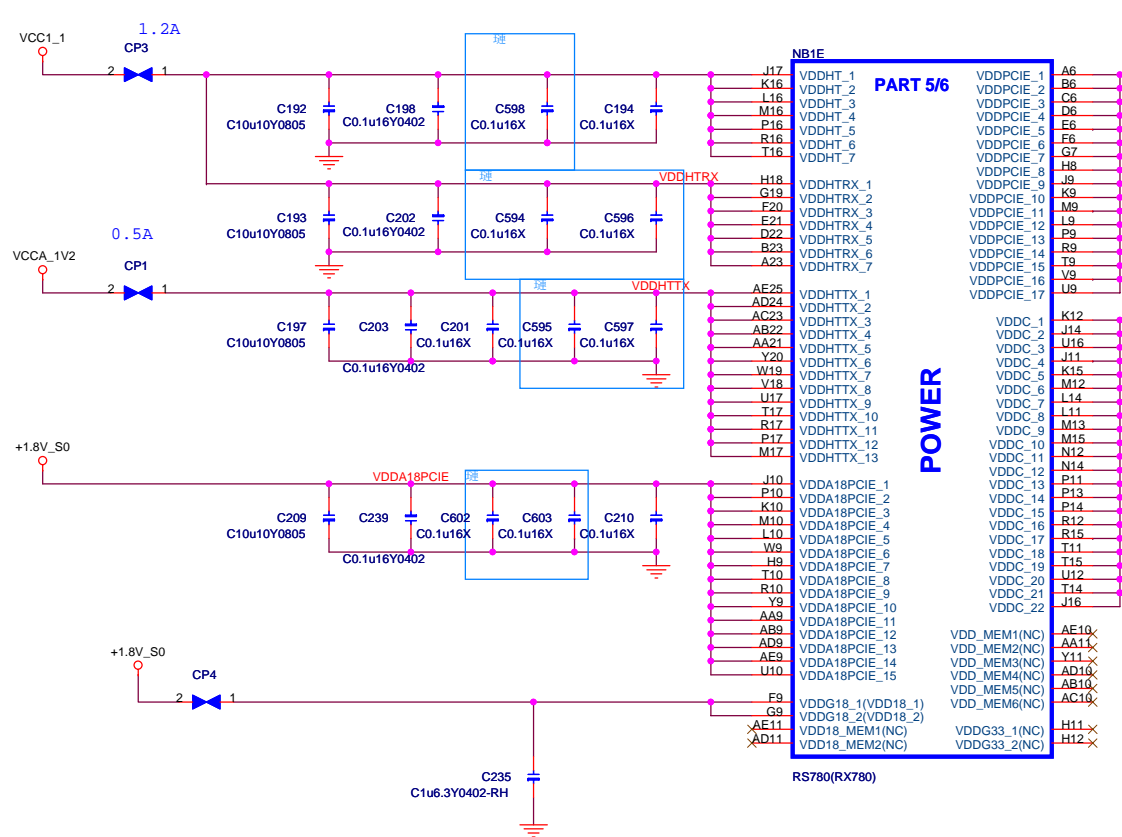
- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVDD18 is connected to 1.8 V and IOPLLVD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.

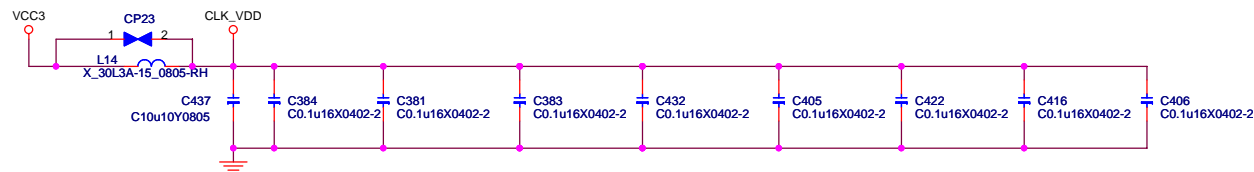
Micro Star Restricted Secret	
Title	Rev
RD780/RX780-HT LINK I/F	0A
Document Number	MS-7599
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RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLT18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLTP33	+3.3V	NC	NC





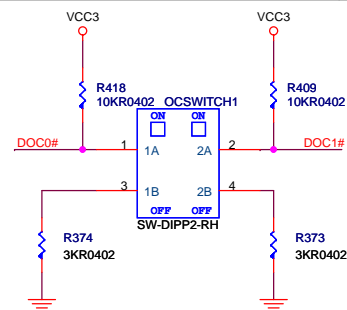
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1- PLACE ALL THE SERIES TERMINATION
RESISTORS AS CLOSE AS U41 AS POSSIBLE

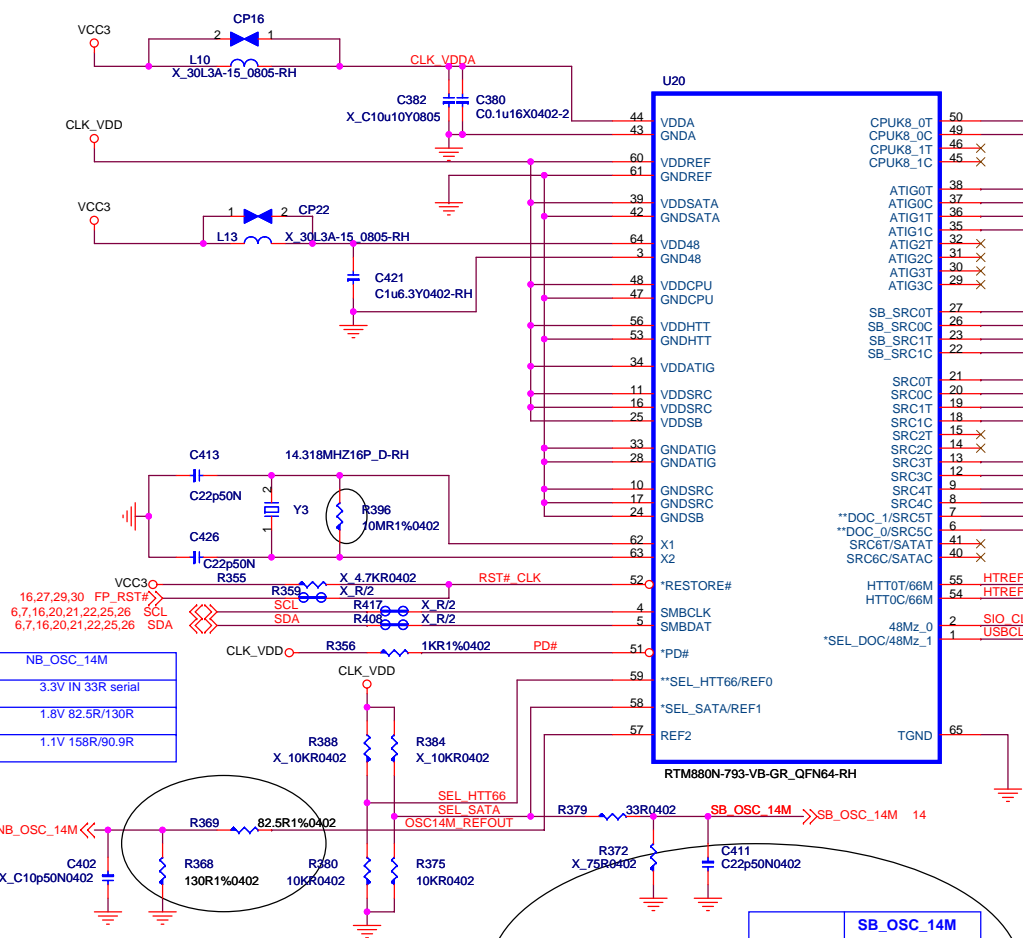
2- ROUTE ALL CPUCLK/#, NBSRCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U41
POWER PIN

```

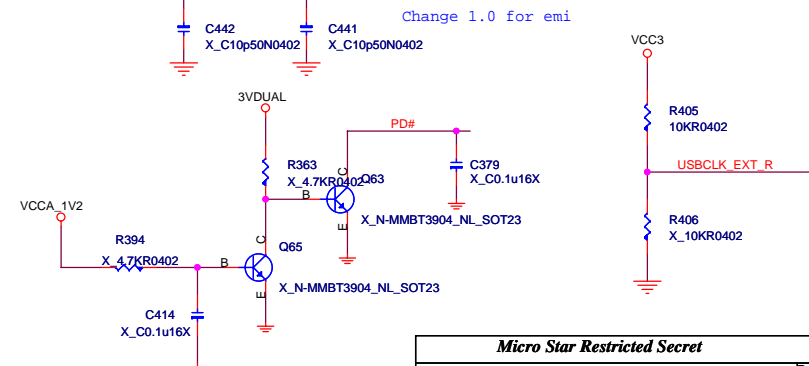


| DOC1 | DOC2 | CPU Frequency                 |
|------|------|-------------------------------|
| 0    | 0    | 200MHZ DEFAULT                |
| 0    | 1    | 250MHZ,{CR07[7:5], CR08[7:0]} |
| 1    | 0    | 300MHZ,{CR14[2:0], CR13[7:0]} |
| 1    | 1    | 350MHZ,{CR1C[2:0], CR15[7:0]} |

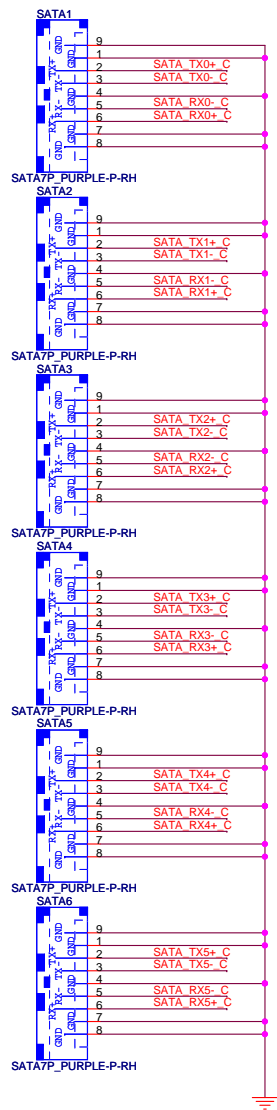


|       | NB_OSC_14M         |
|-------|--------------------|
| RS740 | 3.3V IN 33R serial |
| RX780 | 1.8V 82.5R/130R    |
| RS780 | 1.1V 158R/90.9R    |

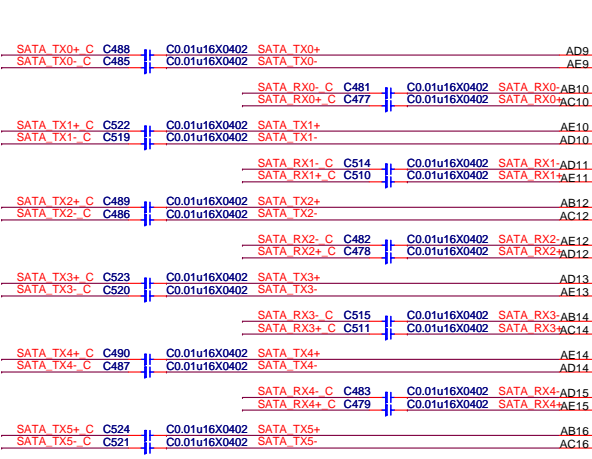
|          |            |
|----------|------------|
|          | SB_OSC_14M |
| SB7XXA13 | 1.2V 110R  |
| SB7XXA14 | 3.3V 33R   |





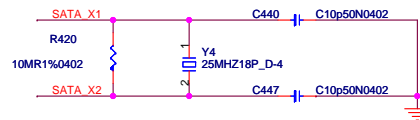


Impedance 90 Ohm, refer to AN\_SB700AB2

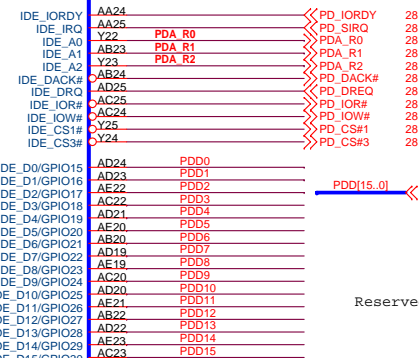
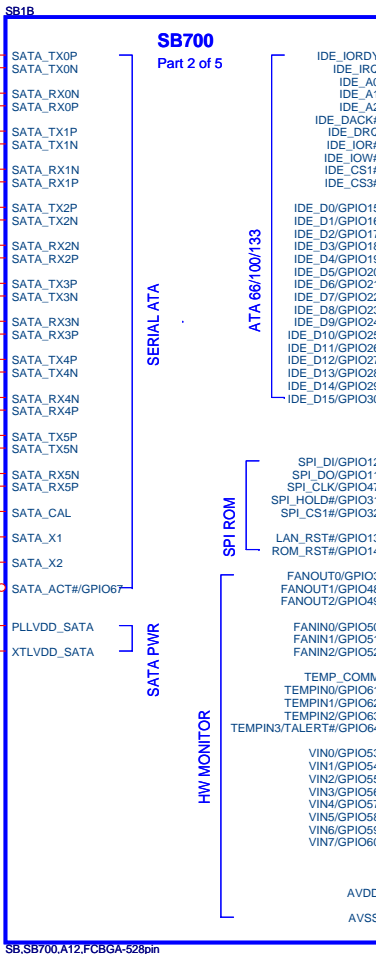
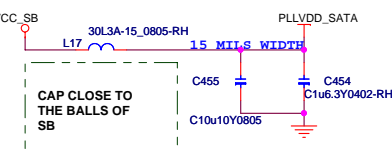
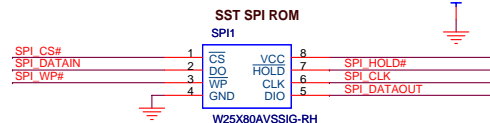
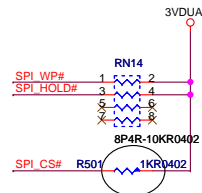


R272 IS 1K 1% FOR XTAL,  
4.99K 1% FOR INTERNAL CLK

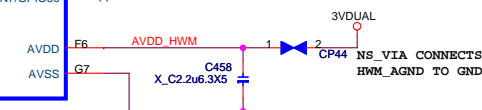
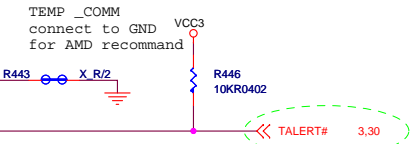
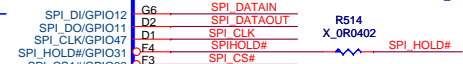
N5N-07M0231-H06



PLLVDV\_SATA -> AA11  
XTLVDD\_SATA -> W12



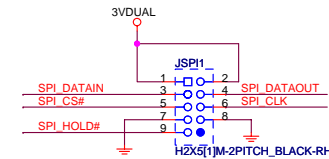
Reserved for EMI 0906



### SPI FLASH MEMORY

### SPI DEBUG PORT

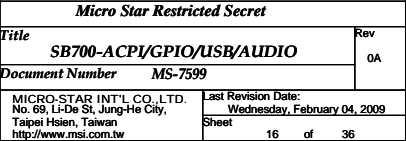
Place close to SPI ROM



Part Number : N31-2051451-H06

| Micro Star Restricted Secret    |                        |          |
|---------------------------------|------------------------|----------|
| Title                           | SB700-SATA/IDE/HWM/SPI | Rev      |
| Document Number                 | MS-7599                | 0A       |
| MICRO-STAR INT'L CO., LTD.      |                        |          |
| No. 69, Li-De St, Jung-He City, |                        |          |
| Taipei Hsien, Taiwan            |                        |          |
| http://www.msi.com.tw           |                        |          |
| Last Revision Date:             |                        | Sheet    |
| Tuesday, February 03, 2009      |                        | 15 of 36 |

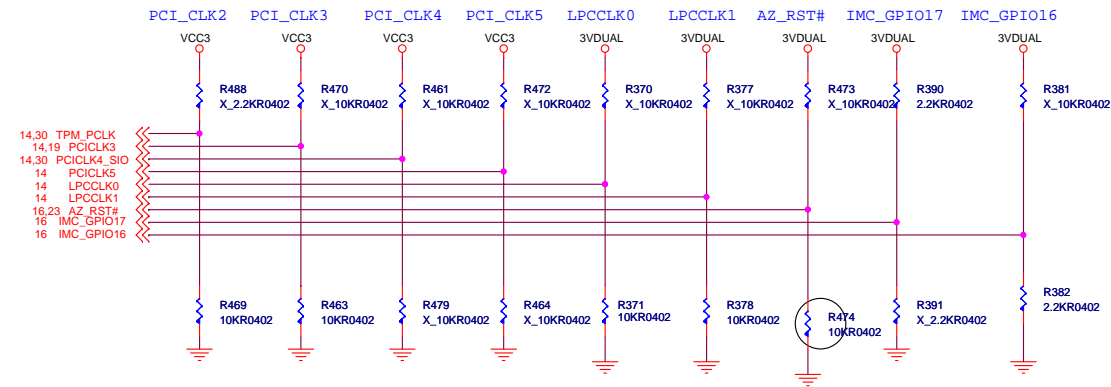






REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK



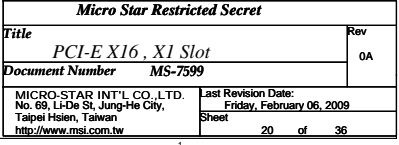
|           | PCI_CLK2                                       | PCI_CLK3                       | PCI_CLK4 | PCI_CLK5 | LPC_CLK0                | LPC_CLK1                   | AZ_RST#                         | IMC_GPIO17                                     | IMC_GPIO16 |
|-----------|------------------------------------------------|--------------------------------|----------|----------|-------------------------|----------------------------|---------------------------------|------------------------------------------------|------------|
| PULL HIGH | WATCHDOG TIMER ON NB_PWRGD ENABLED             | USE DEBUG STRAPS               | RESERVED | RESERVED | IMC ENABLED             | CLKGEN ENABLED             | ENABLE PCI MEM BOOT             | ROM TYPE:<br>H, H = Reserved<br>H, L = SPI ROM |            |
| PULL LOW  | WATCHDOG TIMER ON NB_PWRGD DISABLED<br>DEFAULT | IGNORE DEBUG STRAPS<br>DEFAULT |          |          | IMC DISABLED<br>DEFAULT | CLKGEN DISABLED<br>DEFAULT | DISABLE PCI MEM BOOT<br>DEFAULT | L, H = LPC ROM<br>L, L = FWH ROM               | DEFAULT    |

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[30:23]

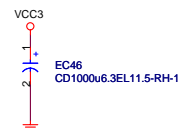
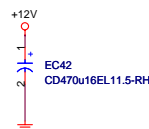
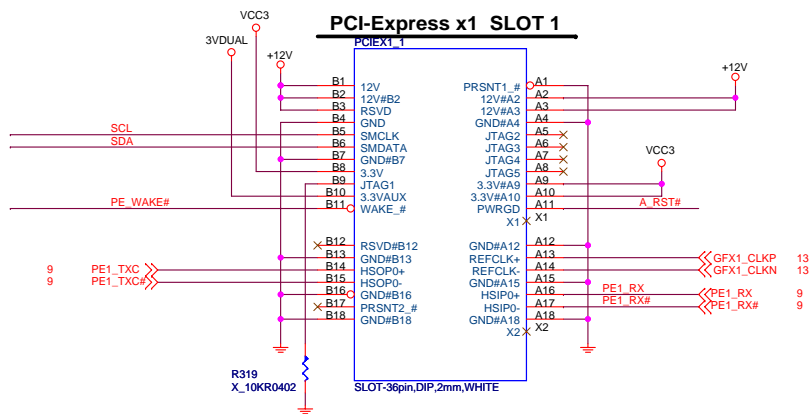
|           | PCI_AD28                  | PCI_AD27               | PCI_AD26                 | PCI_AD25               | PCI_AD24                           | PCI_AD23 |
|-----------|---------------------------|------------------------|--------------------------|------------------------|------------------------------------|----------|
| PULL HIGH | USE LONG RESET<br>DEFAULT | USE PCI PLL<br>DEFAULT | USE ACPI BCLK<br>DEFAULT | USE IDE PLL<br>DEFAULT | USE DEFAULT PCIE STRAPS<br>DEFAULT | RESERVED |
| PULL LOW  | USE SHORT RESET           | BYPASS PCI PLL         | BYPASS ACPI BCLK         | BYPASS IDE PLL         | USE EEPROM PCIE STRAPS             |          |



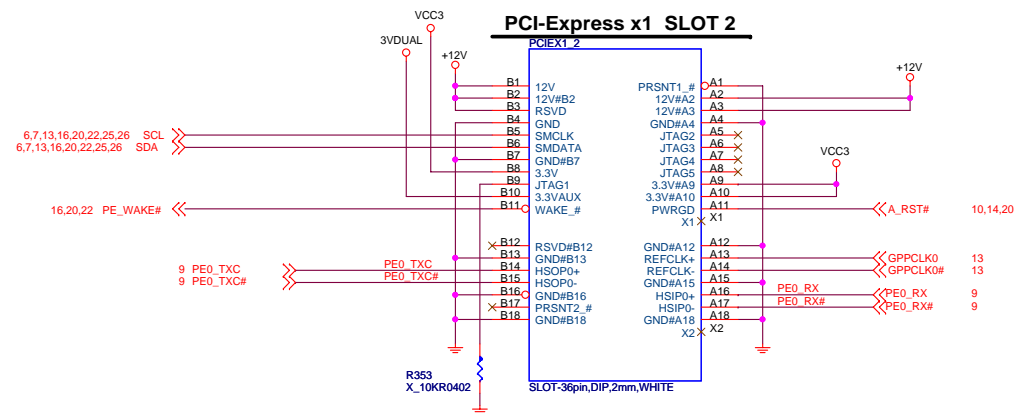


FOR RX780 PCI-EX1

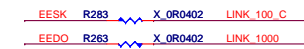
# PCI-Express x1 SLOT 1



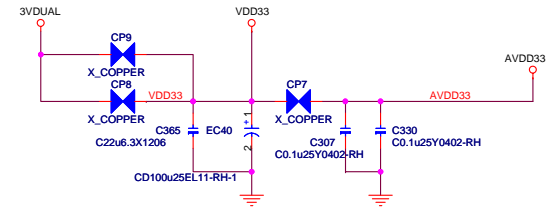
# PCI-Express x1 SLOT 2



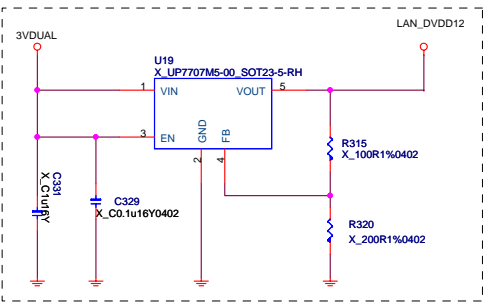
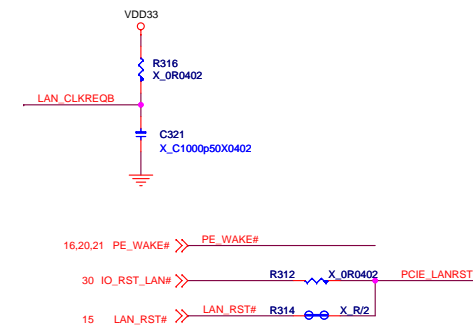
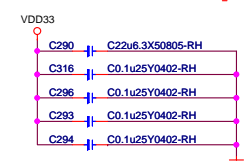
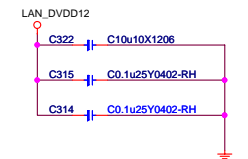
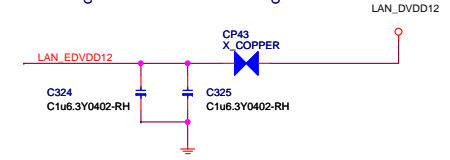
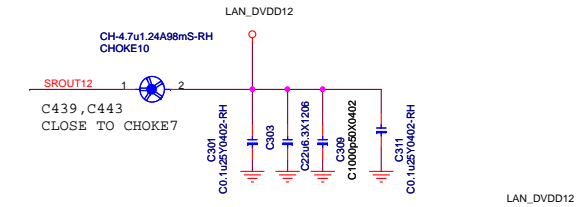
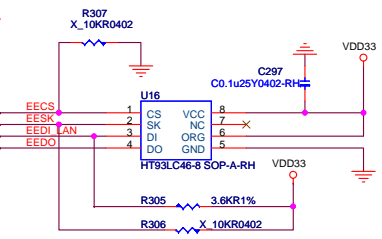
| Micro Star Restricted Secret                                                                                                                       |                    |                                                                       |
|----------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------------------------------------------------------------|
| Title                                                                                                                                              | PCIE X1 Slot 1 , 2 | Rev<br>0A                                                             |
| Document Number                                                                                                                                    | MS-7599            |                                                                       |
| MICRO-STAR INT'L CO., LTD.<br>No. 68, Li-De St, Jung-Ho City,<br>Taipei Hsien, Taiwan<br><a href="http://www.msi.com.tw">http://www.msi.com.tw</a> |                    | Last Revision Date:<br>Friday, February 06, 2009<br>Sheet<br>21 of 36 |



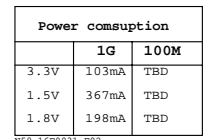
```
High:Enable SW on LAN
LOW:Disable SW on LAN
```



MDIx+/- Reference to GND plan.



|           |  |
|-----------|--|
| RTL8111DL |  |
| 3.3V      |  |
| 3.3V      |  |
| 3.3V      |  |
| 1.2V      |  |
| 1.2V      |  |
| 1.2V      |  |
|           |  |

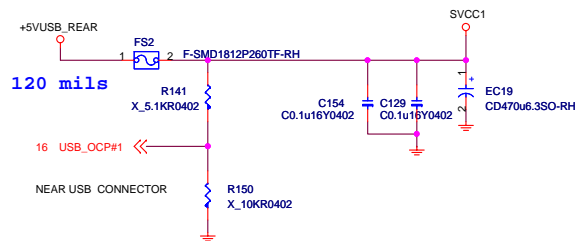


|                                                                                                                                                            |                             |                                                                                                      |
|------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|------------------------------------------------------------------------------------------------------|
| <b>Micro Star Restricted Secret</b>                                                                                                                        |                             |                                                                                                      |
| <b>Title</b>                                                                                                                                               | <b>LAN - Realtek 8111DL</b> | <b>Rev</b>                                                                                           |
| <b>Document Number</b>                                                                                                                                     | <b>MS-7599</b>              | <b>0A</b>                                                                                            |
| <b>MICRO-STAR INT'L CO., LTD.</b><br>No. 68, Li-De St., Jung-Ho City,<br>Taipei Hsien, Taiwan<br><a href="http://www.msi.com.tw">http://www.msi.com.tw</a> |                             | <b>Last Revision Date:</b><br><b>Wednesday, February 04, 2009</b><br><b>Sheet</b> 22      of      36 |

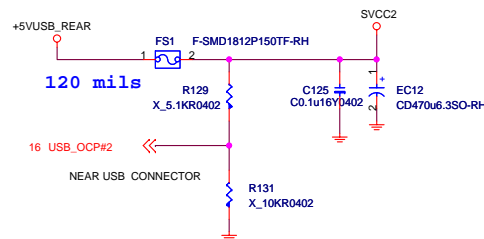




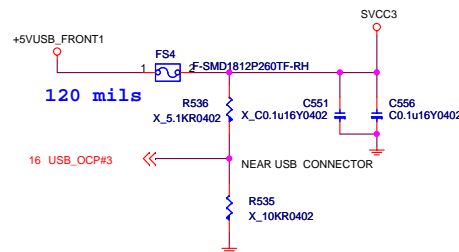
### POWER CIRCUIT FOR USB PORT 0,1,2,3



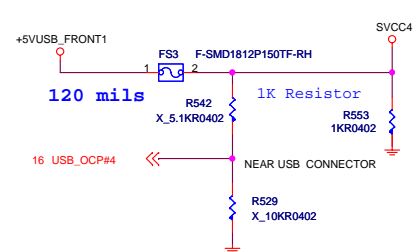
### POWER CIRCUIT FOR USB PORT 4,5



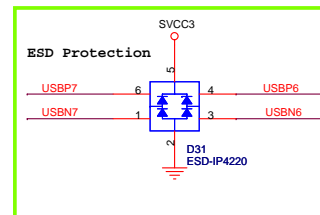
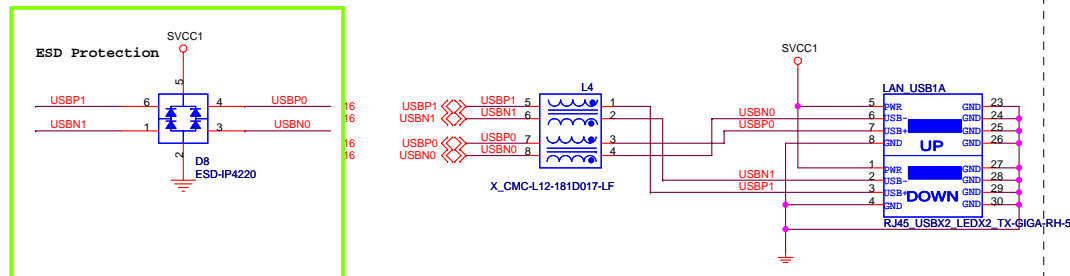
### POWER CIRCUIT FOR USB PORT 6,7,8,9



### POWER CIRCUIT FOR USB PORT 10,11

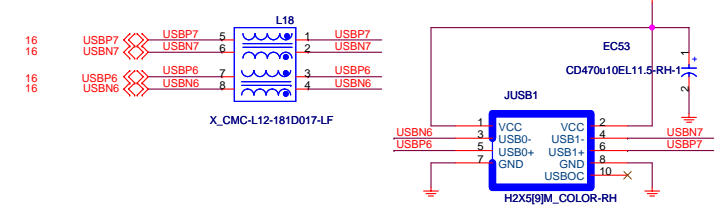


### REAR PANEL USB CONNECTOR FOR USB PORT 0,1

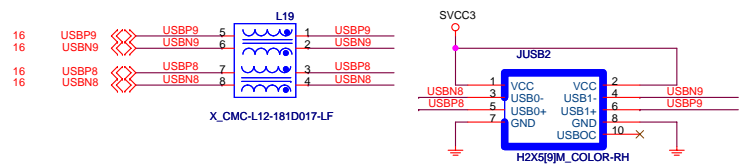


### FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

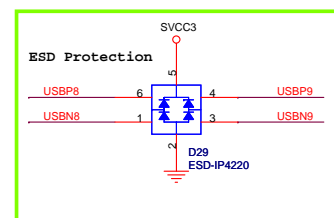
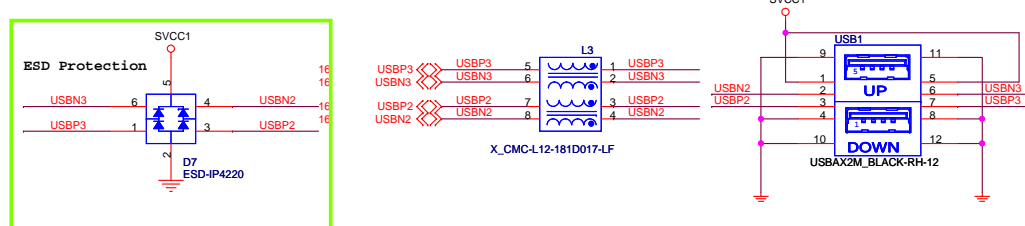
Reversed, can be taken off riser card within bead



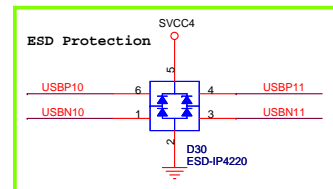
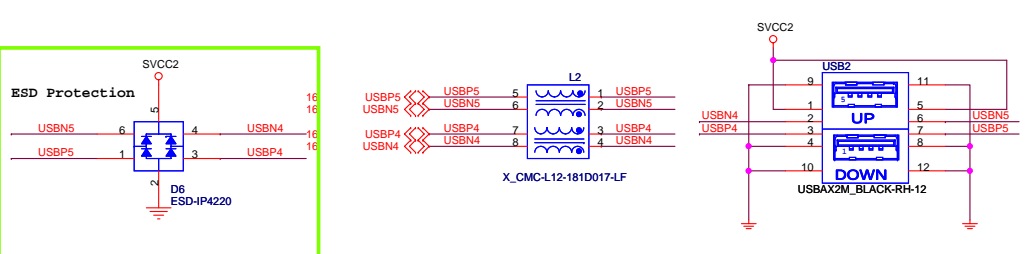
### FRONT PANEL USB CONNECTOR FOR USB PORT 8,9



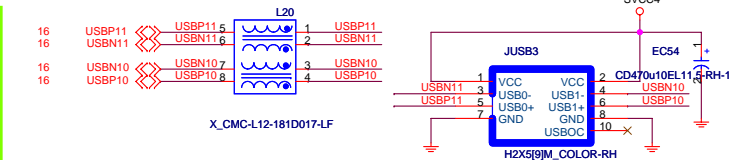
### REAR PANEL USB CONNECTOR FOR USB PORT 2,3



### REAR PANEL USB CONNECTOR FOR USB PORT 4,5

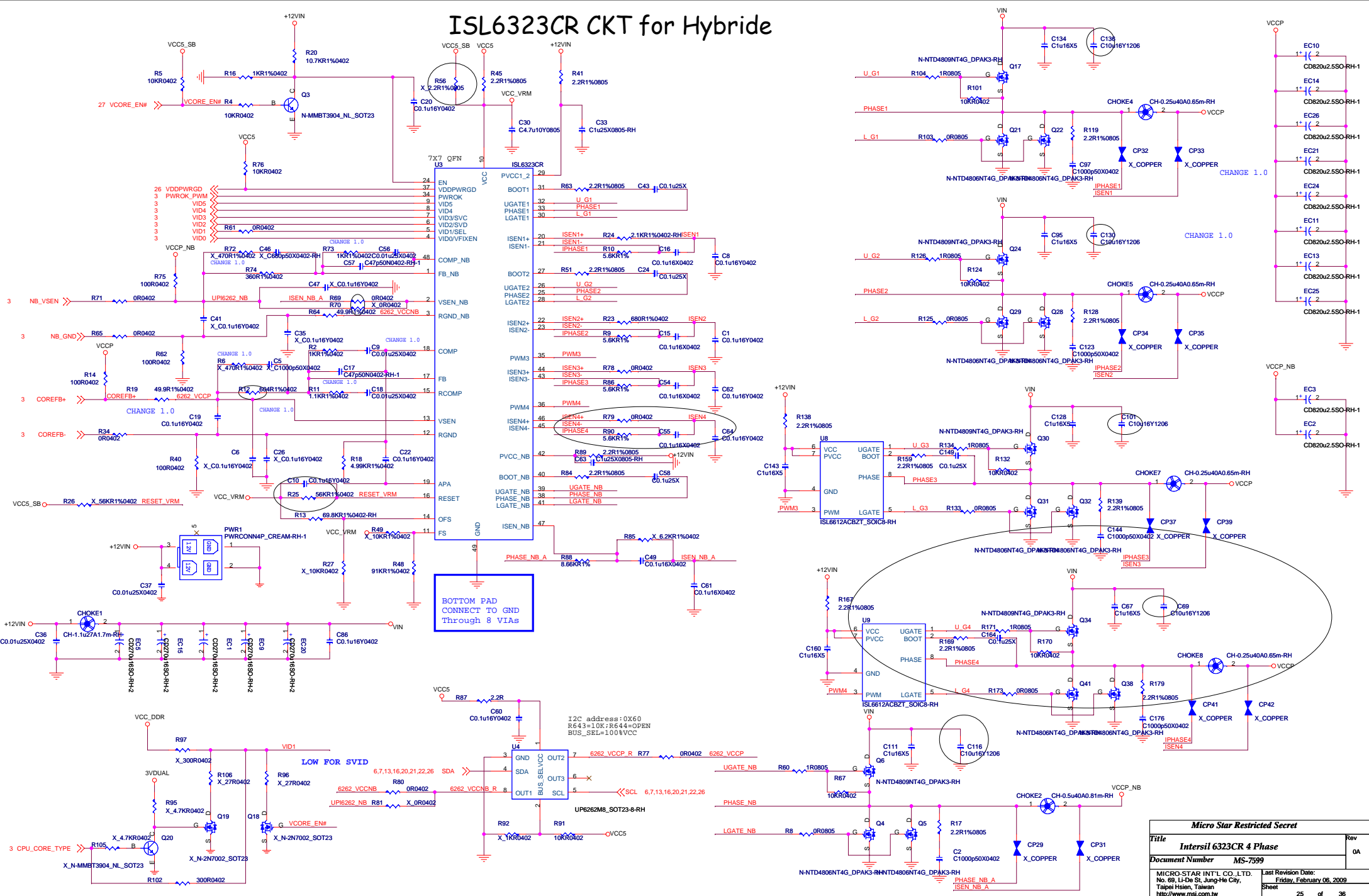


### FRONT PANEL USB CONNECTOR FOR USB PORT 10,11

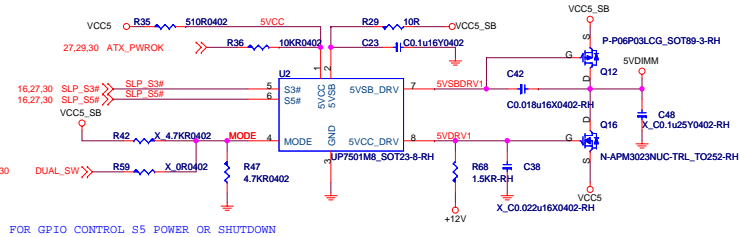


| Micro Star Restricted Secret                                                           |                |                                                  |
|----------------------------------------------------------------------------------------|----------------|--------------------------------------------------|
| Title                                                                                  | USB CONNECTORS | Rev                                              |
| Document Number                                                                        | MS-7599        | 0A                                               |
| MICRO-STAR INT'L CO., LTD.<br>No. 68, Li-De St, Jung-Hsi City,<br>Taipei Hsien, Taiwan |                | Last Revision Date:<br>Monday, February 09, 2009 |
| http://www.msi.com.tw                                                                  |                | Sheet 24 of 36                                   |

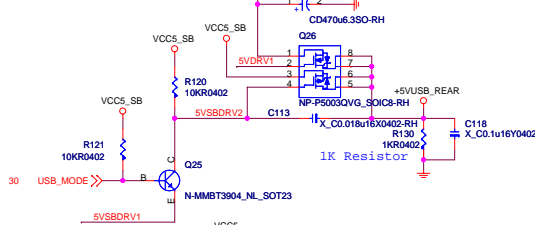
## ISL6323CR CKT for Hybride



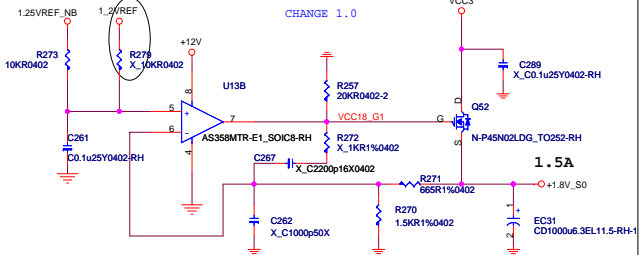
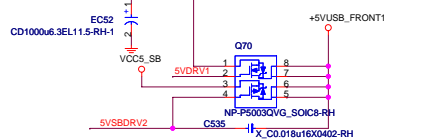
## 5VDIMM FOR DDR



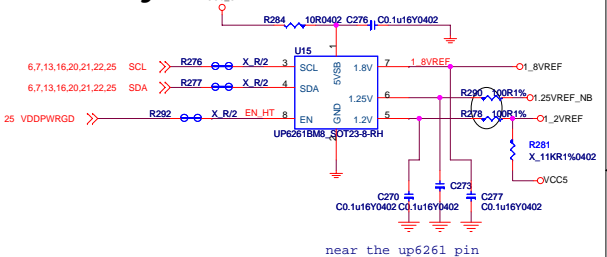
## 5VSB FOR Rear USB



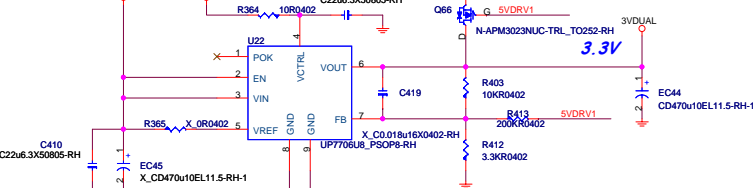
## 5VSB FOR Front USB



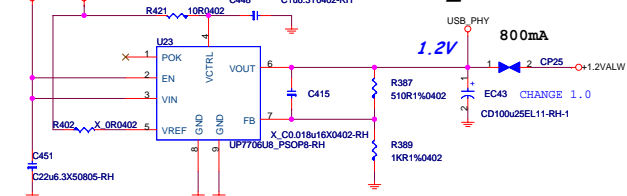
## reference Voltage



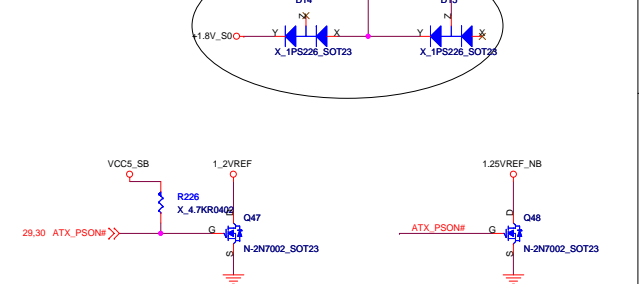
## 3VDUAL

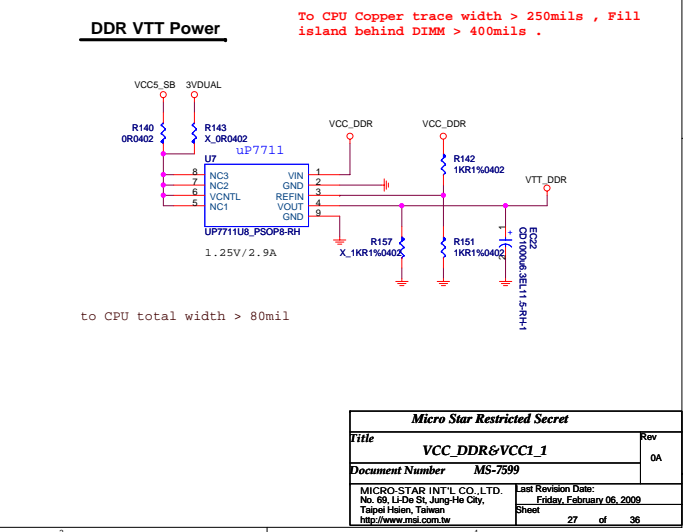
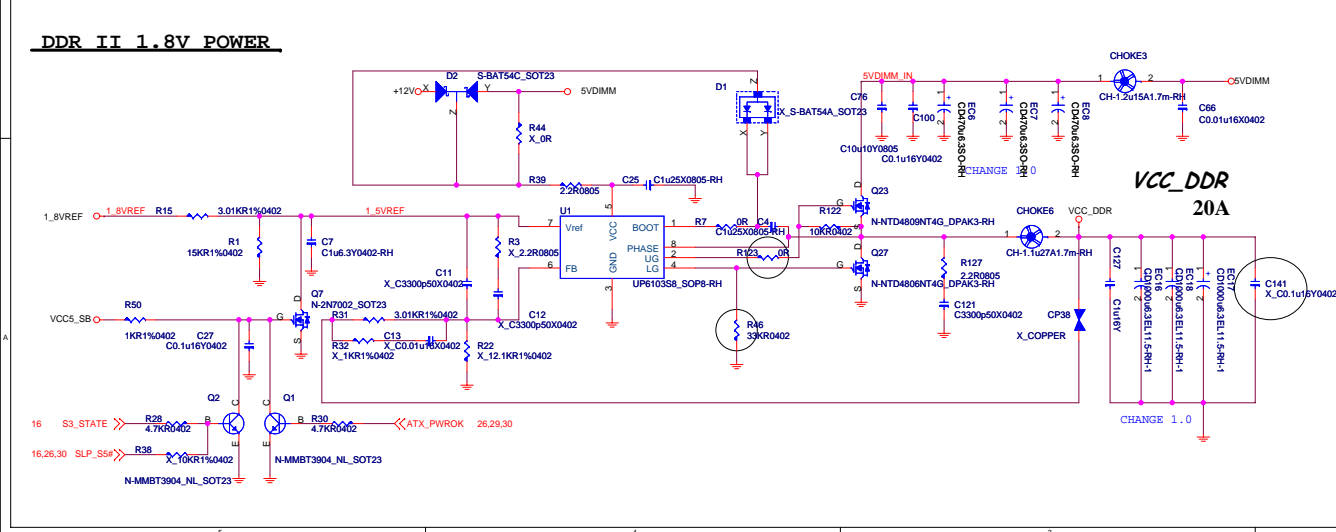
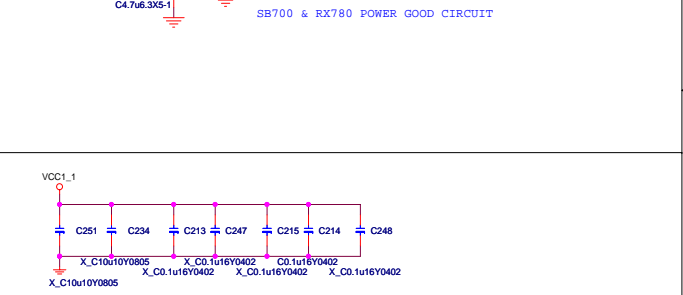
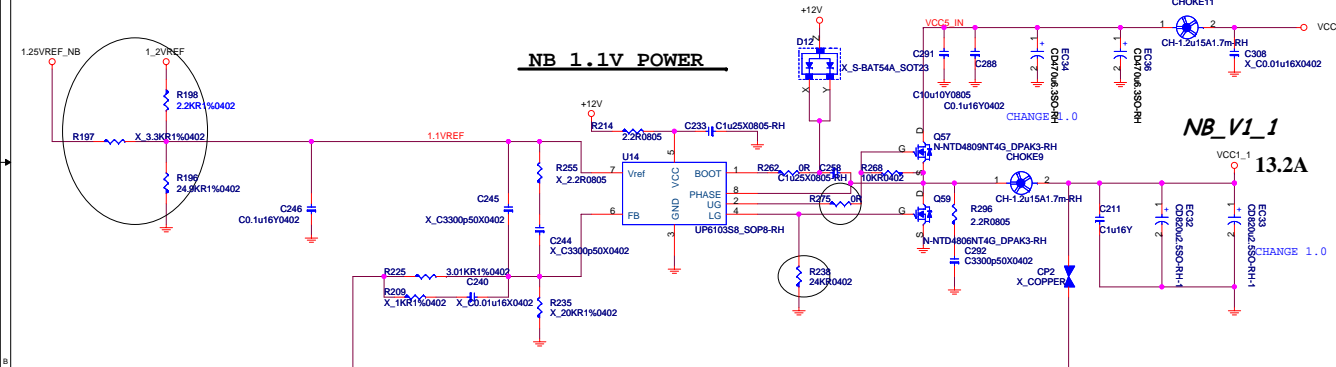
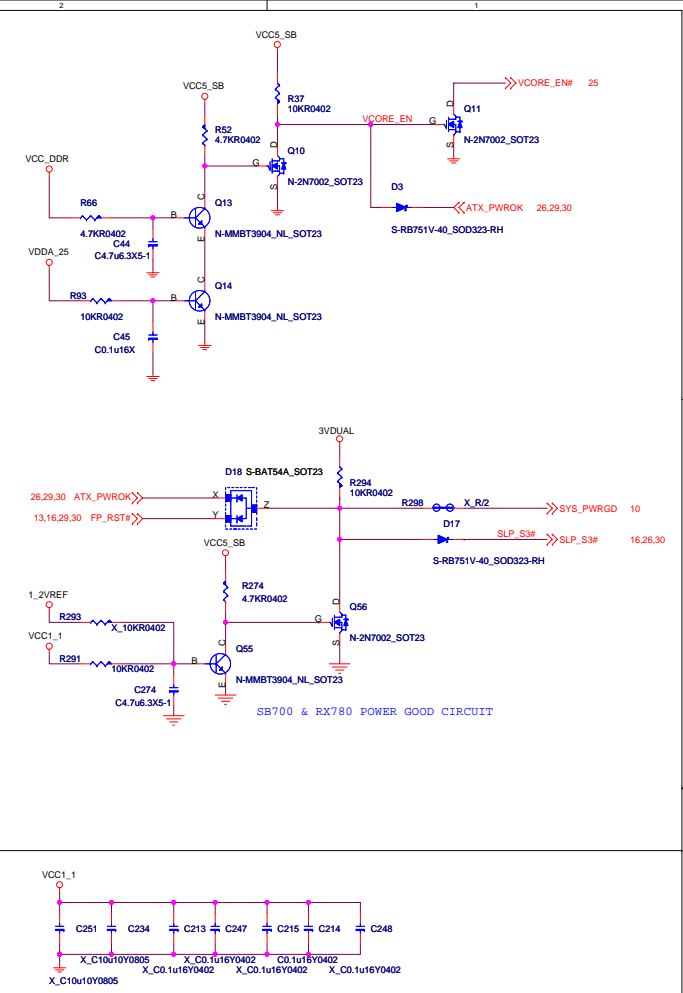
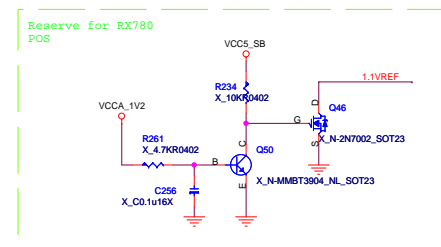
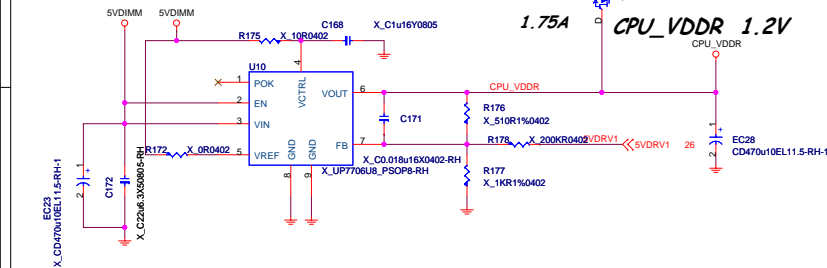
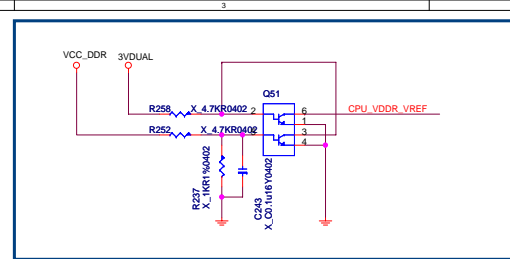
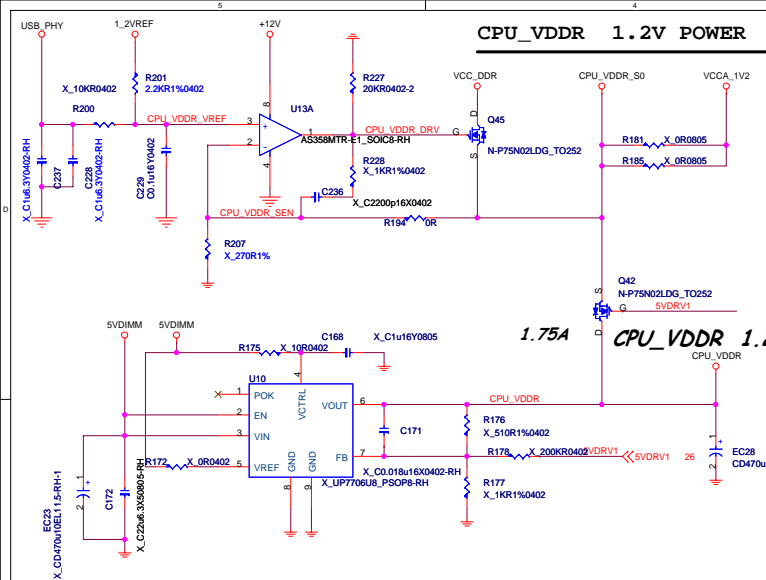


## USB\_PHY

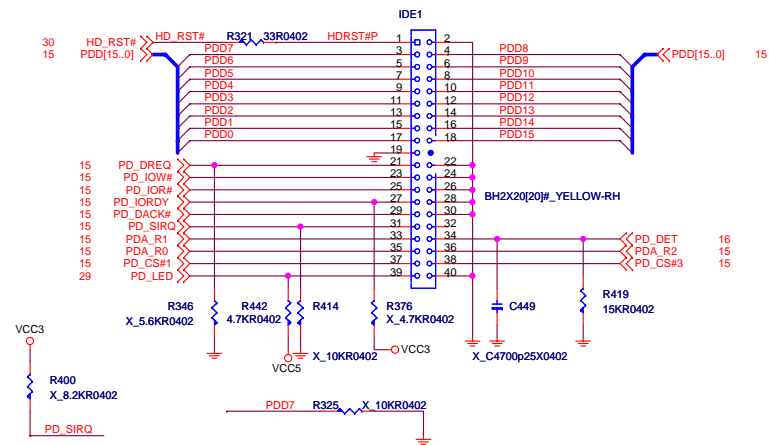


## wide trace





|                                                                                                                |                |                                                                       |
|----------------------------------------------------------------------------------------------------------------|----------------|-----------------------------------------------------------------------|
| Micro Star Restricted Secret                                                                                   |                |                                                                       |
| Title                                                                                                          | VCC_DDR&VCC1_1 | Rev                                                                   |
| Document Number                                                                                                | MS-7599        | 0A                                                                    |
| MICRO-STAR INT'L CO. LTD.<br>No. 89, Li-Joe St, Jung-Ho City,<br>Taipei Hsien, Taiwan<br>http://www.msi.com.tw |                | Last Revision Date:<br>Friday, February 06, 2009<br>Sheet<br>27 of 36 |



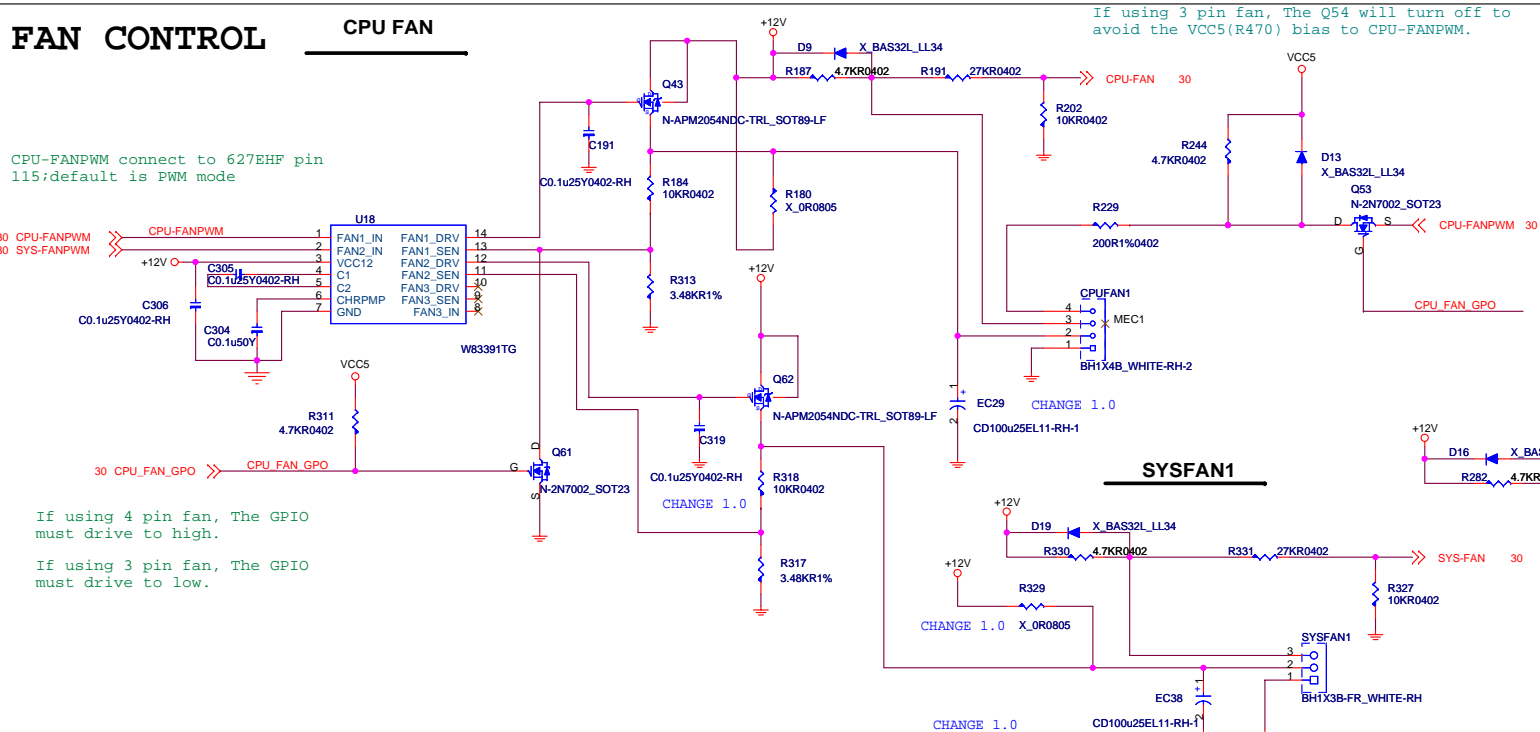
## FAN CONTROL CPU FAN

CPU-FANPWM connect to 627EHF pin 115; default is PWM mode

30 CPU-FANPWM  
30 SYS-FANPWM

If using 4 pin fan, The GPIO must drive to high.

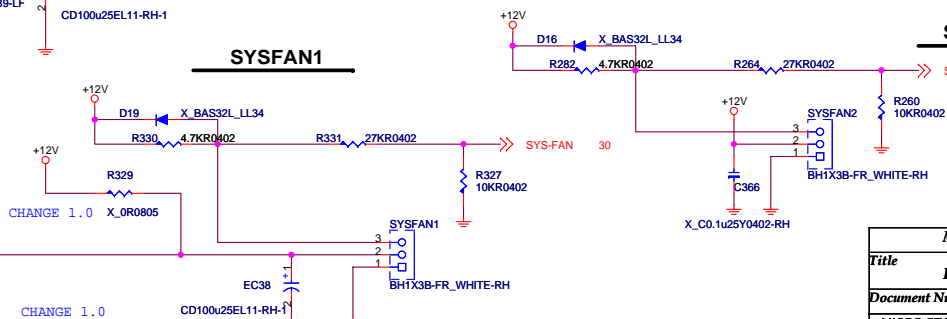
If using 3 pin fan, The GPIO must drive to low.



If using 3 pin fan, The Q54 will turn off to avoid the VCC5(R470) bias to CPU-FANPWM.

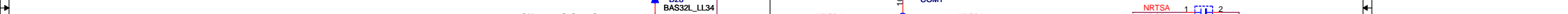
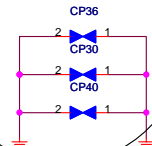
## SYSFAN1

## SYS FAN



| Micro Star Restricted Secret                                                                                                                       |                       |                                                                        |
|----------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|------------------------------------------------------------------------|
| Title                                                                                                                                              | IDE Conn/FAN/LPT/SATA | Rev                                                                    |
| Document Number                                                                                                                                    | MS-7599               | 0A                                                                     |
| MICRO-STAR INT'L CO., LTD.<br>No. 69, Li-De St, Jung-Ho City,<br>Taipei Hsien, Taiwan<br><a href="http://www.msi.com.tw">http://www.msi.com.tw</a> |                       | Last Revision Date:<br>Tuesday, February 03, 2009<br>Sheet<br>28 of 36 |

## Intel Front Panel

[illegible]

**PS2 KEYBOARD & MOUSE CONNECTOR**

This diagram illustrates the internal circuitry of a PS2 Keyboard & Mouse Connector. It shows the connection of the connector pins to the system's data bus and power supply.

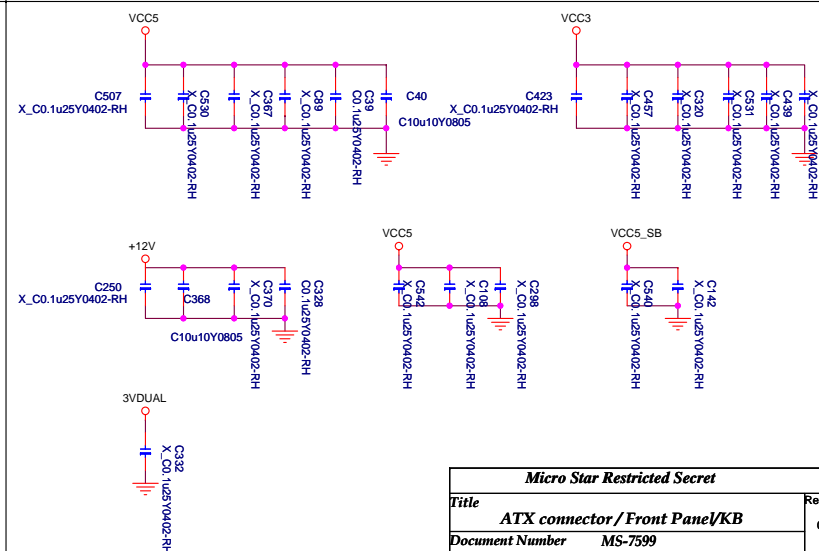
**Components and Connections:**

- SVCC2:** The main power supply input, connected to the VCC pins of the connector.
- MSDATA, MSCLK, KBDATA, KBCLK:** The data and clock signals from the system, connected to the corresponding pins of the connector.
- Capacitors:**
  - C21:** A 100nF capacitor connected to the VCC pin.
  - C29, C30, C31, C34:** 180pF capacitors connected to the data and clock lines.
  - C28:** A 180pF capacitor connected to the ground pin.
- Resistor:**
  - RN1:** An 8P4R-4.7K0402 resistor connected to the VCC pin.
- Connectors:**
  - KB1:** A 16-pin connector for the keyboard.
  - MS:** A 5-pin connector for the mouse.
- MINIDIN12P-RH:** A 12-pin connector for the system's data bus.

### SERIAL PORT 1

The diagram illustrates the wiring for Serial Port 1, centered around the U6 module (GD75232\_SSOP20). The module's pins are connected to various components as follows:

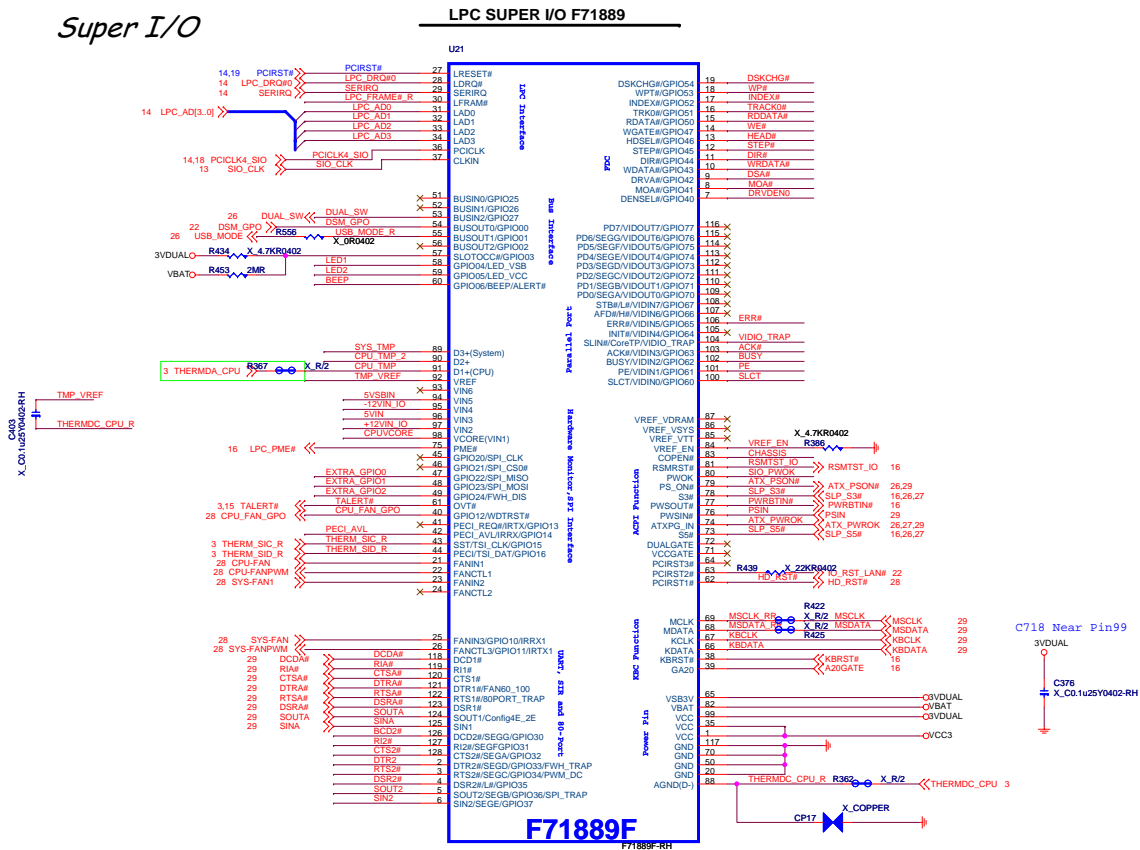
- Power and Ground:**
  - VCC (Pin 1) is connected to +12VCOM.
  - GND (Pin 11) is connected to -12VCOM.
- Signal Lines:**
  - Pin 19 (RIA#) is connected to RIA# (Pin 30).
  - Pin 18 (CTSA#) is connected to CTSA# (Pin 30).
  - Pin 17 (DSRA#) is connected to DSRA# (Pin 30).
  - Pin 14 (SINA) is connected to SINA (Pin 30).
  - Pin 12 (DCDA#) is connected to DCDA# (Pin 30).
  - Pin 5 (NRTSA) is connected to NRTSA (Pin 30).
  - Pin 6 (NDTRA) is connected to NDTRA (Pin 30).
  - Pin 8 (NSOUTA) is connected to NSOUTA (Pin 30).
- Connectors:**
  - COM1:** A 5-pin connector with pins 1-5 connected to NDCDA#, NSINA#, NSOUTA#, NDTRA#, and GND.
  - DSUB-COMM\_GREEN-RH-5:** A 5-pin connector with pins 1-5 connected to NDCDA#, NSINA#, NSOUTA#, NDTRA#, and GND.
- Other Components:**
  - Capacitors C90 and C106 are connected between the +12VCOM and -12VCOM lines.
  - Resistors D4 and D5 are connected between the +12VCOM and -12VCOM lines.



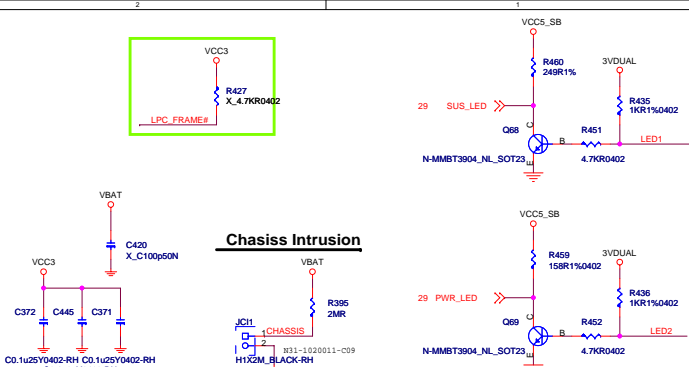
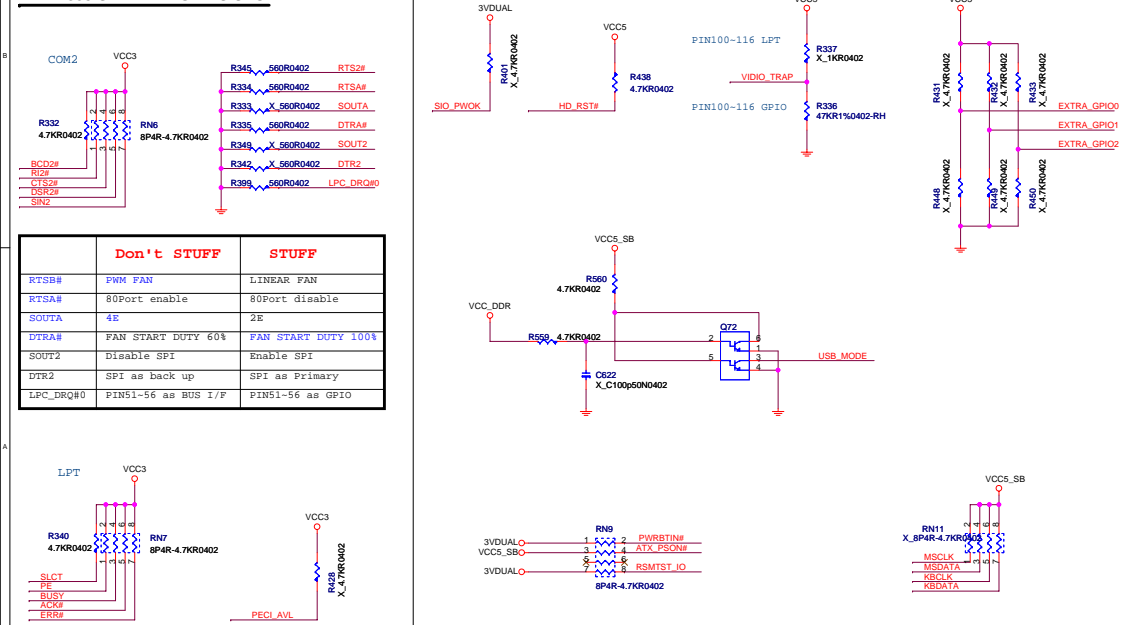
|                                                                                                                                                    |                |                                                                                                   |
|----------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------------------------------------------------------------------------------------------------|
| <b>Micro Star Restricted Secret</b>                                                                                                                |                |                                                                                                   |
| <b>Title</b>                                                                                                                                       | <b>Rev</b>     |                                                                                                   |
| <b>ATX connector / Front Panel/KB</b>                                                                                                              | <b>0A</b>      |                                                                                                   |
| <b>Document Number</b>                                                                                                                             | <b>MS-7599</b> |                                                                                                   |
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*Super I/O*

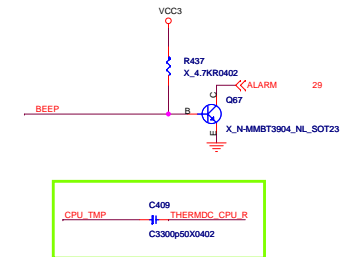


## F71889 STRAPPING RESISTOR

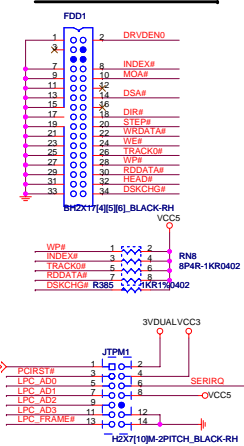


BEEP

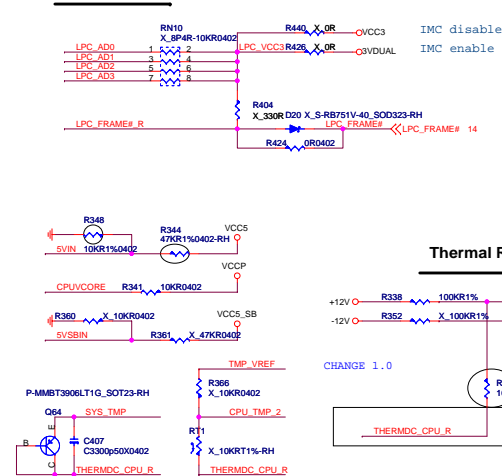
Ver C:Pop R32 and R27 and Q2. non-pop R31  
Ver G,H:Pop R27 and R31. non-pop R32 and Q2



### FLOPPY CONNECTOR

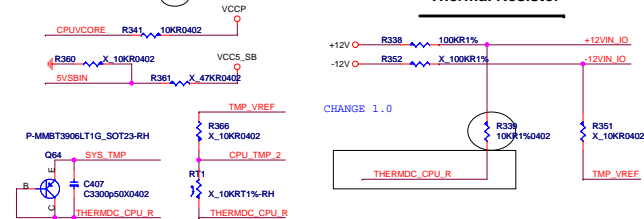


### LPC PULL UP



**NOTE: LOCATE CLOSE  
STATUS PANEL**

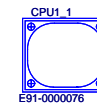
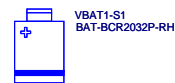
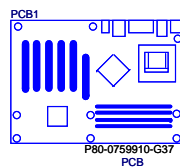
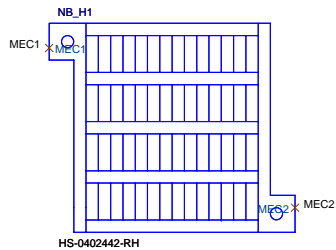
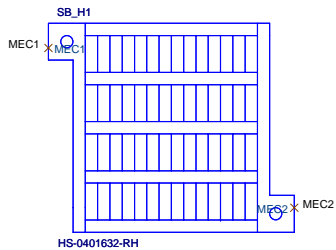
### Thermal Resistor



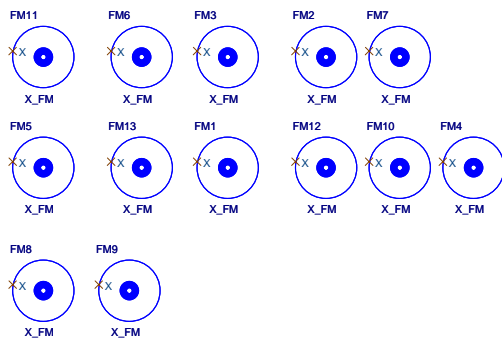
Micro Star Restricted Secret

|       |                                  |
|-------|----------------------------------|
| Title | LPC SUPER I/O & LPC & CONNECTORS |
|-------|----------------------------------|

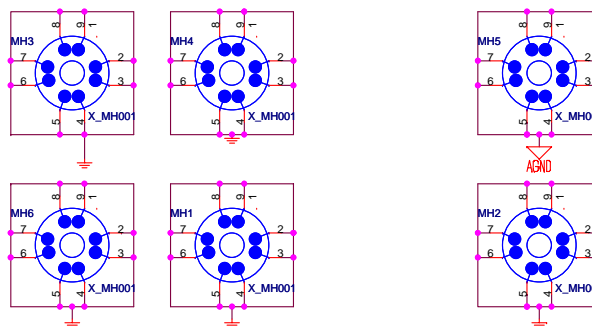
|                                                                                                                                                         |                                                         |
|---------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------|
| <b>Document Number</b> MS-7599                                                                                                                          |                                                         |
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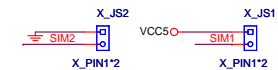
### Optics Orientation Holes



### Mounting Holes

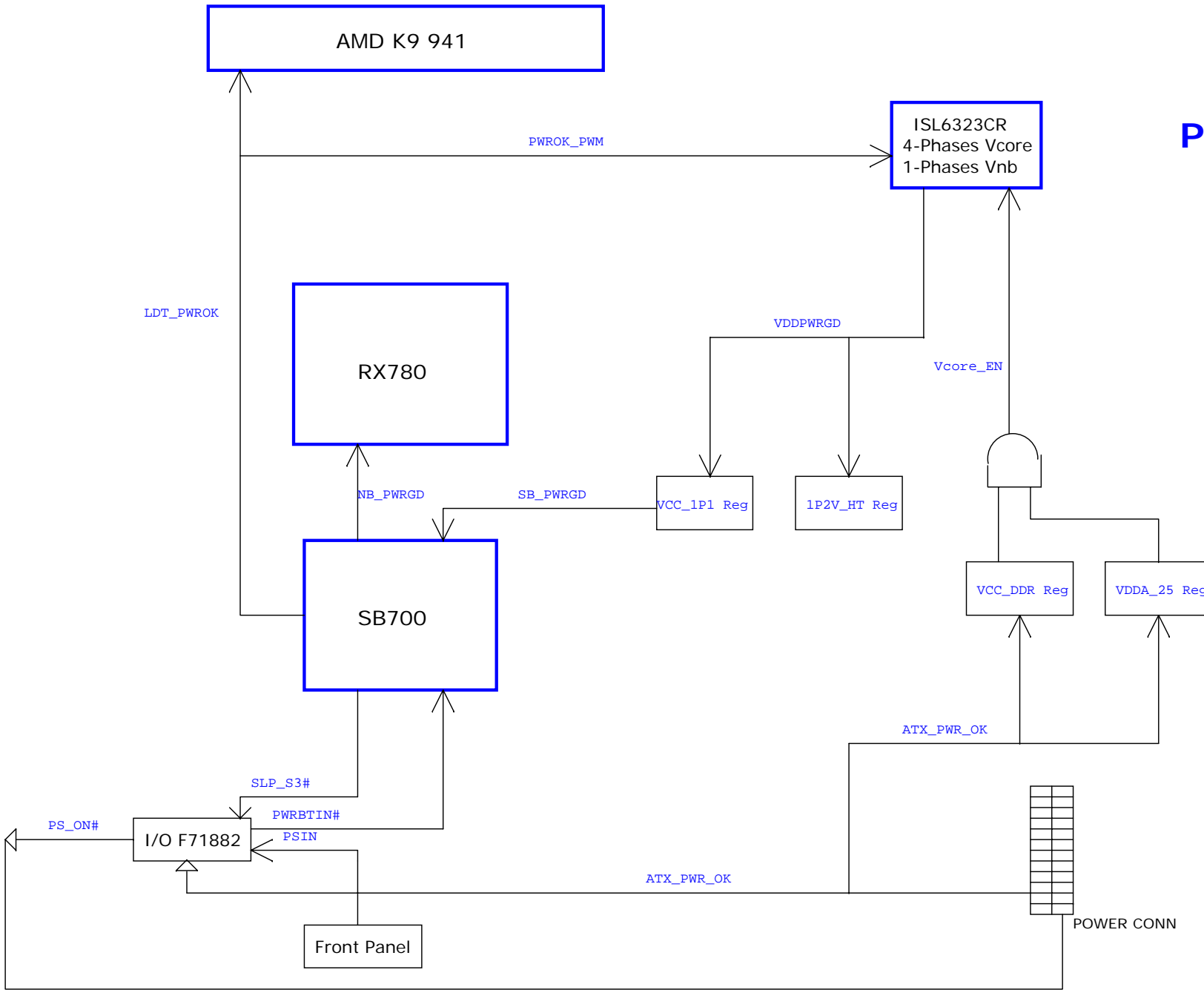


### Simulation



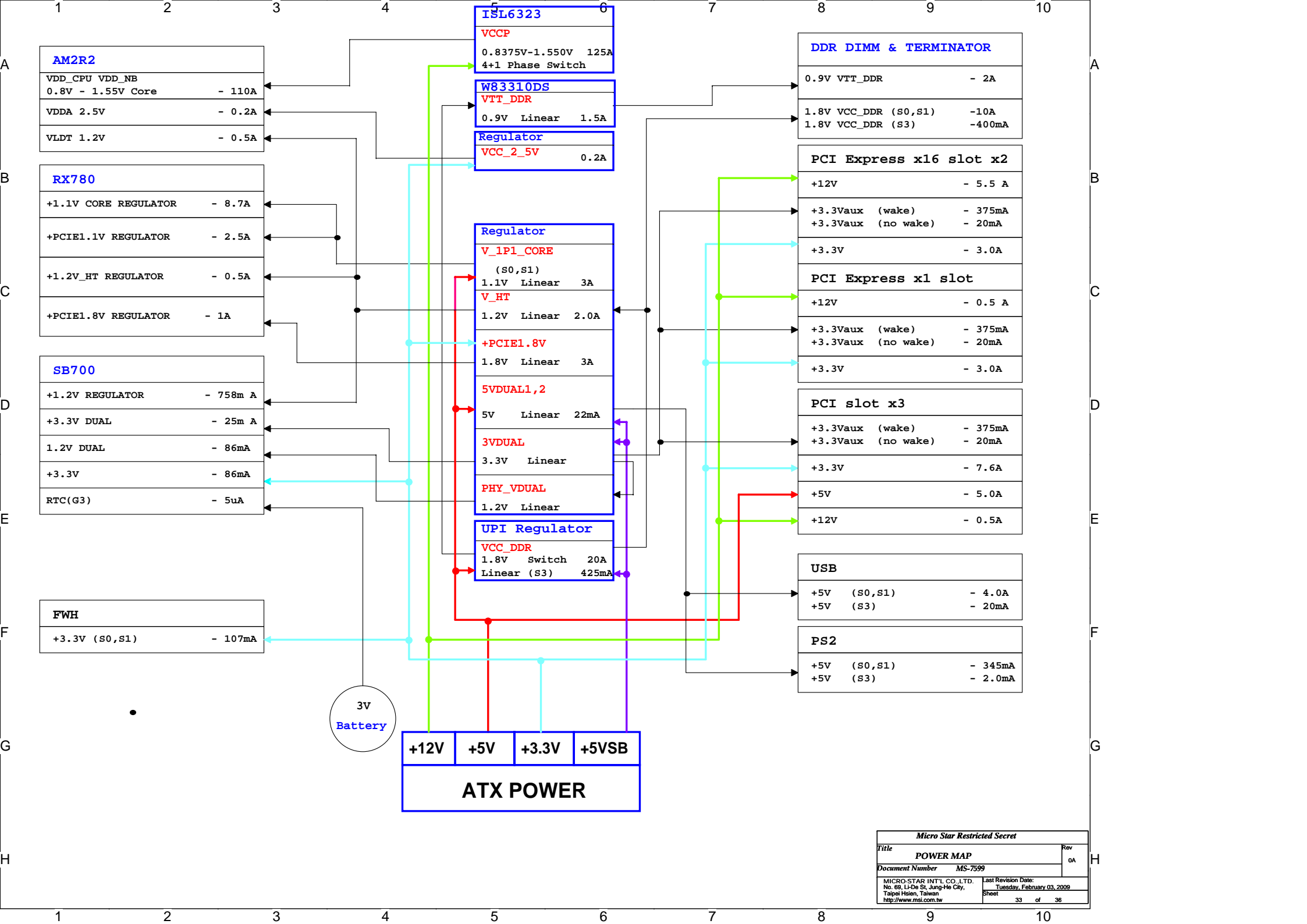
Micro Star Restricted Secret

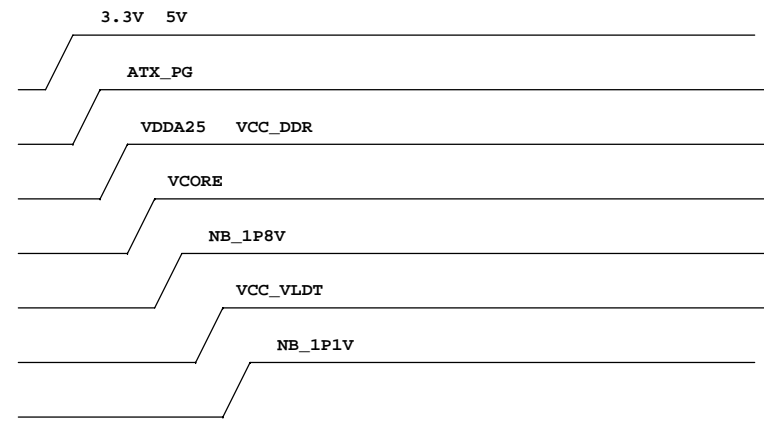
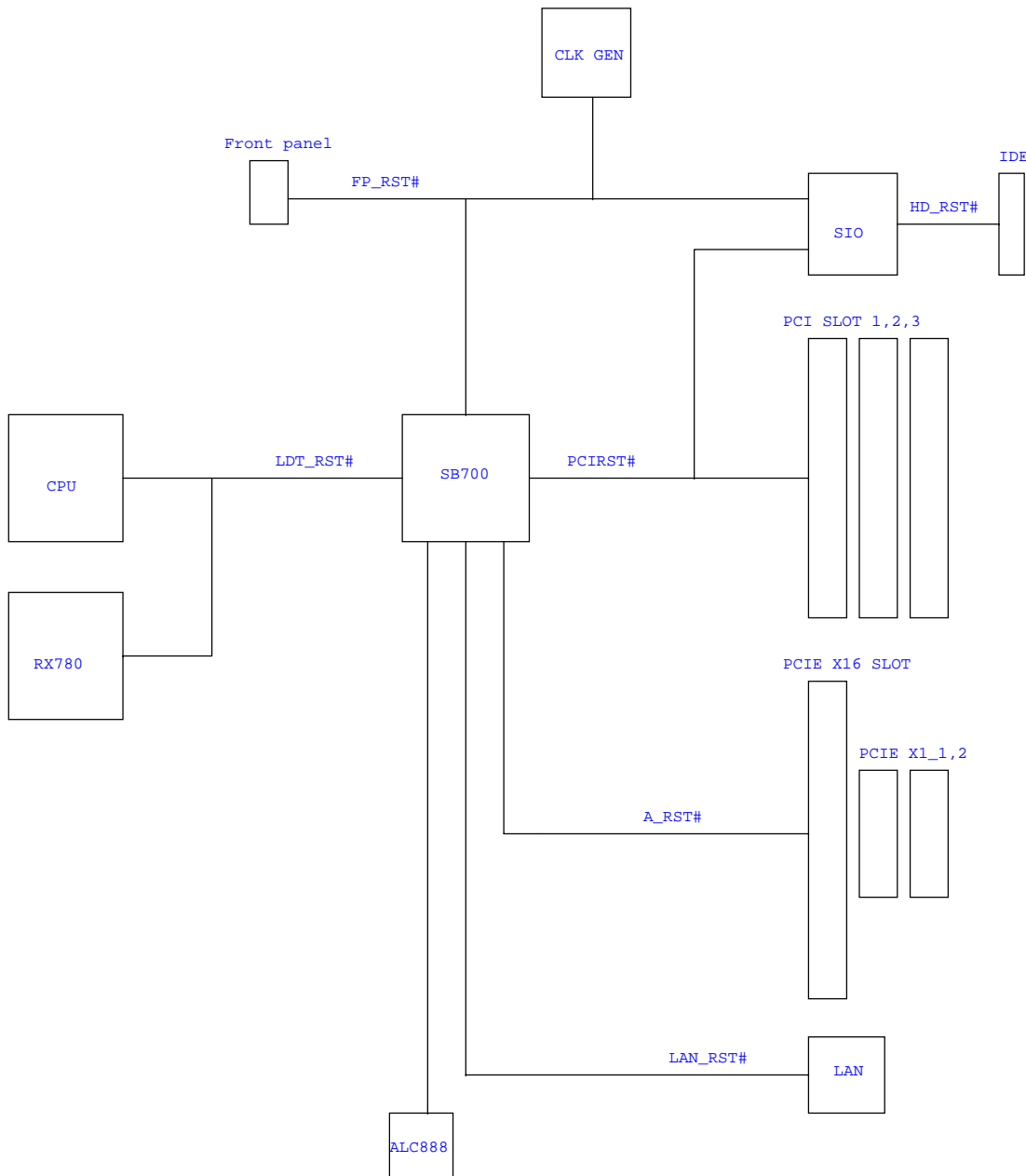
| Title                                                                                                                                              |  | Rev                                                       |
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| MANUAL PARTS                                                                                                                                       |  | 0A                                                        |
| Document Number                                                                                                                                    |  |                                                           |
| MS-7599                                                                                                                                            |  |                                                           |
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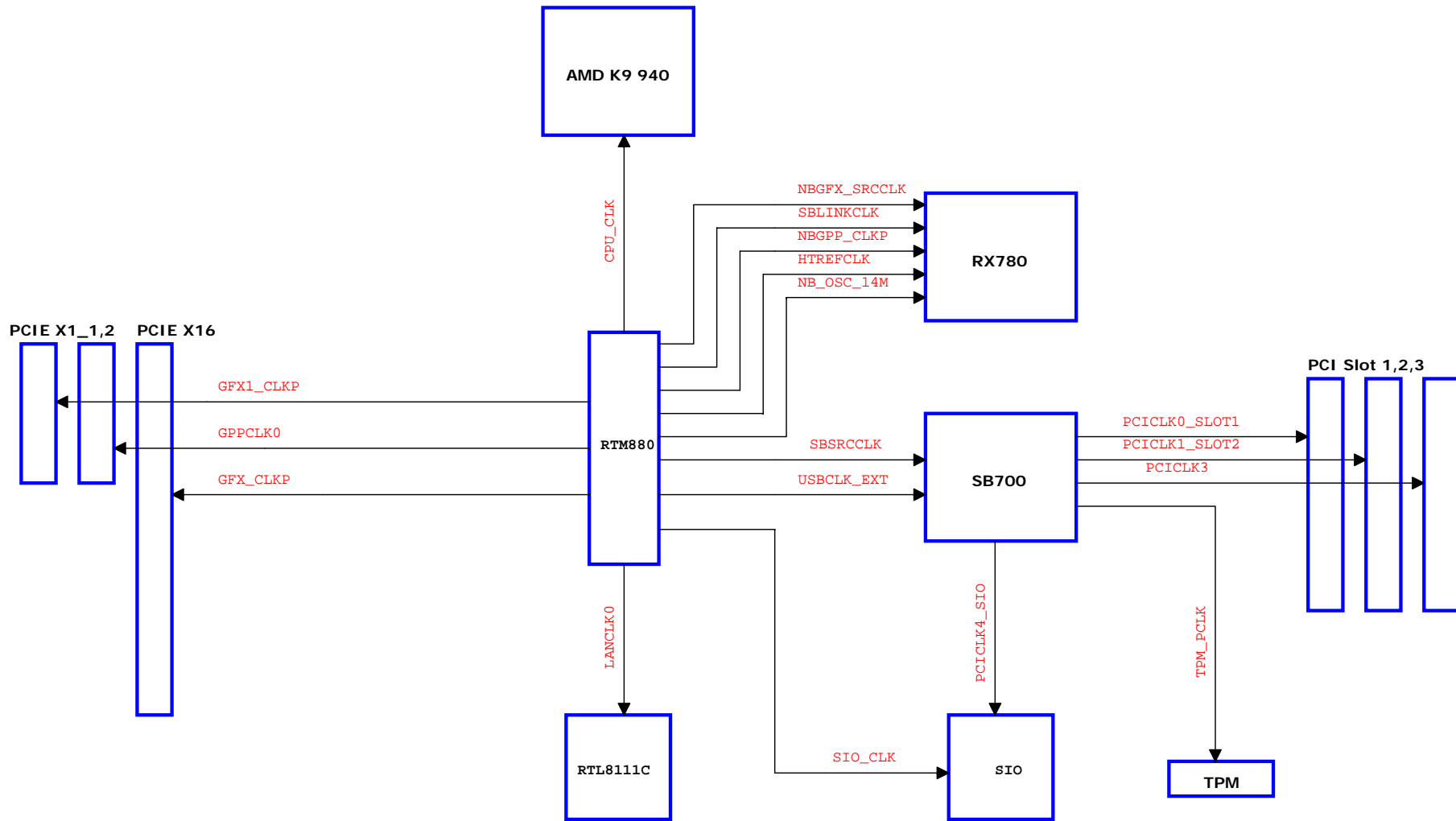
## PWROK MAP

|                                                                                                                                                    |           |                                                            |
|----------------------------------------------------------------------------------------------------------------------------------------------------|-----------|------------------------------------------------------------|
| Micro Star Restricted Secret                                                                                                                       |           |                                                            |
| Title                                                                                                                                              | PWROK MAP | Rev                                                        |
| Document Number                                                                                                                                    | MS-7599   | 0A                                                         |
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| Micro Star Restricted Secret                                                                                                                        |                          |                                                   |
| Title                                                                                                                                               | RESET MAP&Power Sequence | Rev                                               |
| Document Number                                                                                                                                     | MS-7599                  | 0A                                                |
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| Title                                                                                                                                             | Clock Map | Rev                                                                 |
| Document Number                                                                                                                                   | MS-7599   | 0A                                                                  |
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1 add C66  
2 change the C5,C6,C7,C12 ,C29,C30,C31,C32 footprint to 0805  
3 add Q69  
4 add EC53,EC56

|                                                                                                                                                   |                                                   |           |
|---------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|-----------|
| Micro Star Restricted Secret                                                                                                                      |                                                   |           |
| Title                                                                                                                                             | HISTORY                                           | Rev<br>0A |
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